```
Set     Items   Description
S1         84   AU='THOMPSON C' OR AU='THOMPSON C L'
S2          6   AU='THOMPSON CAROL L'
S3          1   AU='LITTFIN J'
S4         90   S1 OR S2 OR S3
S5         39   S4 AND IC=G06F?
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
         (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/May W01
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040513,UT=20040506
         (c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200431
         (c) 2004  Thomson Derwent
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5/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07428889 **Image available**
METHOD FOR GIVING ϕ FUNCTION FOR PERFORMING STATIC SINGLE SUBSTITUTION

PUB. NO.: 2002-297399 [JP 2002297399 A]
PUBLISHED: October 11, 2002 (20021011)
INVENTOR(s): **THOMPSON CAROL L**
SANTHANAM VATSA
JU DZ-CHING
BALA VASANTH
APPLICANT(s): HEWLETT PACKARD CO (HP)
APPL. NO.: 2002-018235 [JP 200218235]
FILED: January 28, 2002 (20020128)
PRIORITY: 01 814511 [US 2001814511], US (United States of America), March 22, 2001 (20010322)
INTL CLASS: **G06F-009/45**

ABSTRACT

PROBLEM TO BE SOLVED: To perform static single substitution when a code with predicate exists.
SOLUTION: Guards placed in the individual source operands of a ϕ function show conditions where the corresponding source operands are effective and can be precisely embodied after code reordering. The guards show a basic block being the source of a side which is correlated to the source operand with respect to a control function ϕc showing the confluence of reached effective definitions in the junction of control flow graphs. A ϕc operand is made into a group with the source basic block of the inputted effective side along the operand. The operands are ordered in the phase order of blocks on the operands. When a predicate code exists, a predicate ϕ function ϕp supplies a mechanism for performing SSA. The ϕ function can precisely be embodied after code reordering. The guard of the source operand shows the predicate where the corresponding operand is defined with respect to ϕp.

5/5/2 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01153600
Method and system for correlating profile data dynamically generated from an optimized executable program with source code statements
Verfahren und Anordnung zur Korrelation von Profildaten dynamisch erzeugt durch ein optimiertes ausfuhrbares Programm mit Quellcodeanweisungen
Methode et systeme pour correler des donnees de profil generees dynamiquement depuis un programme executable optimise avec commandes de code source
PATENT ASSIGNEE:
Hewlett-Packard Company, A Delaware Corporation, (3016020), 3000 Hanover Street, Palo Alto, CA 94304, (US), (Proprietor designated states: all)
INVENTOR:
Buzbee, William B., 404 Casa Del Mar Drive, Half Moon Bay, CA 94019, (US)
Ruscetta, Michelle A., 4436 Belvedere Drive, San Jose, CA 95129, (US)
Thompson, Carol L. , 6937 Calabazos Creek Circle, San Jose, CA 95129, (US
LEGAL REPRESENTATIVE:
Tollett, Ian et al (86292), Williams Powell Morley House 26-30 Holborn Viaduct, London EC1A 2BP, (GB)
PATENT (CC, No, Kind, Date): EP 1004961 A2 000531 (Basic)
EP 1004961 A3 010530
EP 1004961 B1 030730

APPLICATION (CC, No, Date): EP 99308943 991110;
PRIORITY (CC, No, Date): US 190994 981112
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-009/45**
CITED PATENTS (EP B): US 5768592 A
CITED REFERENCES (EP B):
CONTE T M ET AL: "ACCURATE AND PRACTICAL-DRIVEN COMPILATION USING THE PROFILE BUFFER" PROCEEDINGS OF THE ANNUAL IEEE/ACM INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE. (MICRO),US,LOS ALAMITOS, IEEE COMP. SOC. PRESS, vol. SYMP. 29, 2 December 1996 (1996-12-02), pages 36-45, XP000724359 ISBN: 0-8186-7641-8.
CHANG P P ET AL: "USING PROFILE INFORMATION TO ASSIST CLASSIC CODE OPTIMIZATIONS" SOFTWARE PRACTICE & EXPERIENCE,GB,JOHN WILEY & SONS LTD. CHICHESTER, vol. 21, no. 12, 1 December 1991 (1991-12-01), pages 1301-1321, XP000276453 ISSN: 0038-0644;

ABSTRACT EP 1004961 A2
A method and system for relating profile data (700) generated by monitoring the execution of an optimized machine-code computer program (600) back to the source-language description. (400) of the computer program. Logical line numbers (604) are associated with the basic blocks (606, 607, 608) of the intermediate-code representation (600) of the computer program and actual line numbers (602) are associated with each instruction (610, 612, 614, 616) of the intermediate-code representation of the computer program. During optimization of the intermediate code, the logical line numbers remain fixed to basic blocks, while actual line numbers remain fixed to intermediate-code instructions. A branch instruction (610) and the target of the branch instruction (612) in the optimized machine-code computer program or in an optimized assembly-language computer program (600) can be related back to source-language statements (400) by using the actual line number (602) associated with the branch instruction (610) and the logical line number (604) associated with the basic block (618) that contains the target of the branch instruction.
ABSTRACT WORD COUNT: 167
NOTE:
Figure number on first page: NONE

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	000531	A2	Published application without search report
Assignee:	010502	A2	Transfer of rights to new applicant: Hewlett-Packard Company, A Delaware Corporation (3016020) 3000 Hanover Street Palo Alto, CA 94304 US
Search Report:	010530	A3	Separate publication of the search report
Examination:	011219	A2	Date of request for examination: 20011022
Examination:	020612	A2	Date of dispatch of the first examination report: 20020425
Change:	030312	A2	Title of invention (German) changed: 20030123
Change:	030312	A2	Title of invention (English) changed: 20030123
Change:	030312	A2	Title of invention (French) changed: 20030123
Grant:	030730	B1	Granted patent

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200022	877
CLAIMS B	(English)	200331	932
CLAIMS B	(German)	200331	892
CLAIMS B	(French)	200331	1036
SPEC A	(English)	200022	6715
SPEC B	(English)	200331	7127
Total word count - document A			7593
Total word count - document B			9987
Total word count - documents A + B			17580

5/5/3 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01046088

COMPUTER ARCHITECTURE FOR THE DEFERRAL OF EXCEPTIONS OF STATICAL SPECULATIVE INSTRUCTIONS

RECHNERARCHITEKTUR ZUR AUFSCHIEBUNG VON EXCEPTIONS STATISCHER SPEKULATIVER BEFEHLE

ARCHITECTURE DE MACHINE POUR LE RETARD D'EXCEPTIONS DES INSTRUCTIONS SPECULATIVES STATIQUES

PATENT ASSIGNEE:
Institute for the Development of Emerging Architectures, L.L.C., (2746711), 19111 Pruneridge Avenue, M/S 44L18, Cupertino, CA 95014-0795, (US), (Proprietor designated states: all)

INVENTOR:
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HAYS, James, O., 1722 Campbell Avenue, San Jose, CA 95125, (US)
BURGER, Stephen, G., 2257 Forbes Avenue, Santa Clara, CA 95050, (US)
MORRIS, Dale, C., 422 Gilbert Avenue, Menlo Park, CA 94025, (US)
THOMPSON, Carol, L. , 6937 Calabazos Creek Circle, San Jose, CA 95129, (US)
GUPTA, Rajiv, 1616 Randolph Parkway, Los Altos, CA 94024, (US)
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HAMMOND, Gary, 519 Sunnybrook Drive, Campbell, CA 95008, (US)
KLING, Ralph, M., 1422 Bedford Avenue, Sunnyvale, CA 94087, (US

LEGAL REPRESENTATIVE:
Jackson, Richard Eric (62281), Carpmaels & Ransford, 43 Bloomsbury Square, London WC1A 2RA, (GB)

PATENT (CC, No, Kind, Date): EP 951672 A1 991027 (Basic)
EP 951672 B1 030219
WO 99019794 990422

APPLICATION (CC, No, Date): EP 98952242 981009; WO 98US21454 981009

PRIORITY (CC, No, Date): US 949295 971013

DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: **G06F-009/38**

CITED PATENTS (EP B): EP 484033 A; GB 2294341 A; US 5201043 A; US 5666508 A

CITED PATENTS (WO A): EP 484033 A ; GB 2294341 A ; US 5666508 A

NOTE:
No A-document published by EPO

LEGAL STATUS (Type, Pub Date, Kind, Text):

Examination:	011004 A1	Date of dispatch of the first examination report: 20010816
Application:	990623 A1	International application (Art. 158(1))
Lapse:	040303 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20030219, BE 20030219, CH 20030219, LI 20030219, DK 20030519, ES 20030828, FI 20030219, GR 20030219, NL 20030219, PT 20030519, SE 20030519,
Lapse:	040121 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20030219, CH 20030219, LI 20030219, DK 20030519, ES 20030828, FI 20030219, GR 20030219, NL 20030219, PT 20030519, SE 20030519,
Lapse:	031119 B1	Date of lapse of European Patent in a contracting state (Country, date): AT 20030219, CH 20030219, LI 20030219, FI 20030219, GR 20030219, NL 20030219, PT 20030519, SE 20030519,
Lapse:	031022 B1	Date of lapse of European Patent in a contracting state (Country, date): CH 20030219, LI 20030219, FI 20030219, NL

20030219, PT 20030519, SE 20030519,
Lapse: 031001 B1 Date of lapse of European Patent in a contracting state (Country, date): CH 20030219, LI 20030219, SE 20030519,
Grant: 030219 B1 Granted patent
Change: 020724 A1 Title of invention (German) changed: 20020605
Change: 020724 A1 Title of invention (English) changed: 20020605
Change: 020724 A1 Title of invention (French) changed: 20020605
Lapse: 030806 B1 Date of lapse of European Patent in a contracting state (Country, date): SE 20030519,
Lapse: 031008 B1 Date of lapse of European Patent in a contracting state (Country, date): CH 20030219, LI 20030219, FI 20030219, NL 20030219, SE 20030519,
Lapse: 031112 B1 Date of lapse of European Patent in a contracting state (Country, date): CH 20030219, LI 20030219, FI 20030219, GR 20030219, NL 20030219, PT 20030519, SE 20030519,
Lapse: 040107 B1 Date of lapse of European Patent in a contracting state (Country, date): AT 20030219, CH 20030219, LI 20030219, DK 20030519, FI 20030219, GR 20030219, NL 20030219, PT 20030519, SE 20030519,
Oppn None: 040211 B1 No opposition filed: 20031120
Application: 991027 A1 Published application with search report
Examination: 991027 A1 Date of request for examination: 19990712
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200308	509
CLAIMS B	(German)	200308	523
CLAIMS B	(French)	200308	517
SPEC B	(English)	200308	7798
Total word count - document A			0
Total word count - document B			9347
Total word count - documents A + B			9347

5/5/4 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01041609
METHOD AND APPARATUS FOR TRANSFERRING DATA BETWEEN A REGISTER STACK AND A MEMORY RESOURCE
VERFAHREN UND GERAT ZUM TRASFERIEREN VON DATEN ZWISCHEN EINEM REGISTERSTAPEL UND EINER SPEICHERQUELLE
PROCEDE ET APPAREIL SERVANT A TRANSFERER LES DONNEES ENTRE UNE PILE DE REGISTRES ET UNE RESSOURCE MEMOIRE
PATENT ASSIGNEE:
Idea Corporation, (2462610), 19447 Pruneridge Avenue, Cupertino, CA 95014 , (US), (Applicant designated States: all)
INVENTOR:
ROSS, Jonathan, K., 974 Lorne Way, Sunnyvale, CA 94087, (US)
COUTANT, Cary, A., 13478 Briar Court, Saratoga, CA 95070, (US)
THOMPSON, Carol, L. , 6937 Calabazas Creek Circle, San Jose, CA 95129, (US)
ZAHIR, Achmed, R., 428 Glenwood Avenue, Menlo Park, CA 94025, (US
LEGAL REPRESENTATIVE:
Kirschner, Klaus Dieter, Dipl.-Phys. et al (6507), Schneiders & Behrendt Rechtsanwalte - Patentanwalte Sollner Strasse 38, 81479 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1019829 A1 000719 (Basic)
WO 9917207 990408
APPLICATION (CC, No, Date): EP 98949726 980930; WO 98US20746 980930
PRIORITY (CC, No, Date): US 940834 970930

DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: **G06F-012/02**
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 000719 A1 Published application with search report
Application: 990609 A1 International application (Art. 158(1))
Change: 040303 A1 Title of invention (German) changed: 20040116
Change: 030416 A1 International Patent Classification changed: 20030221
Change: 030416 A1 International Patent Classification changed: 20030221
Search Report: 030416 A1 Date of drawing up and dispatch of supplementary:search report 20030227
Examination: 000719 A1 Date of request for examination: 20000428
Examination: 030820 A1 Date of dispatch of the first examination report: 20030708
LANGUAGE (Publication,Procedural,Application): English; English; English

5/5/5 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00488442 **Image available**
COMPUTER ARCHITECTURE FOR THE DEFERRAL OF EXCEPTIONS ON SPECULATIVE INSTRUCTIONS
ARCHITECTURE DE MACHINE POUVANT REALISER UN REPORT D'EXCEPTIONS DANS DES INSTRUCTIONS SPECULATIVES
Patent Applicant/Assignee:
INSTITUTE FOR THE DEVELOPMENT OF EMERGING ARCHITECTURES L L C,
Inventor(s):
ROSS Jonathan K,
MILLS Jack D,
HAYS James O,
BURGER Stephen G,
MORRIS Dale C,
THOMPSON Carol L ,
GUPTA Rajiv,
FREUDENBERGER Stefan M,
HAMMOND Gary,
KLING Ralph M
Patent and Priority Information (Country, Number, Date):
Patent: WO 9919794 A1 19990422
Application: WO 98US21454 19981009 (PCT/WO US9821454)
Priority Application: US 97949295 19971013
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: **G06F-009/38**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 8913

English Abstract
The inventive system (300) and method allows for software control (320) of hardware (330) deferral of exceptions in speculative operations (104), and comprises three components. The first component is processor stored information (107) which reflects the code generation strategy of applications and is used by hardware and the operating system to control exception deferral. The second component is processor stored information

(105) set by the operating system to specify to hardware which type of faults should be automatically deferred. The third component is further processor stored information (102) which indicates to the hardware to defer certain exception causing aspects of the speculative operation, while performing other non excepting aspects of the speculative operation. The stored information is set after the operating system exception handler (200) has unsuccessfully attempted fault resolution (213).

French Abstract

Le systeme (300) de l'invention et son procede permettent de controler par logiciel (320) des reports d'exceptions machine (330) dans des operations speculatives (104) et comprennent trois elements. Le premier element (107) est une information stockee en memoire centrale refletant la strategie de generation de code d'applications, et mise en oeuvre par la machine et le systeme d'exploitation pour controler le report d'exceptions. Le deuxieme element (105) est une information stockee en memoire centrale instauree par le systeme d'exploitation pour indiquer a la machine quel type d'erreur doit etre automatiquement reporte. Le troisieme element (102) est egalement une information stockee en memoire centrale qui indique a la machine de differer certains aspects de l'operation speculative qui sont causes d'exceptions mais de realiser en meme temps d'autres aspects de l'operation speculative qui ne sont pas causes d'exceptions. L'information stockee est instauree apres que le gestionnaire d'exception (200) du systeme d'exploitation ait effectue une tentative reussie de resolution d'une erreur (213).

5/5/6 (Item 2 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

00485855 **Image available**

METHOD AND APPARATUS FOR TRANSFERRING DATA BETWEEN A REGISTER STACK AND A MEMORY RESOURCE

PROCEDE ET APPAREIL SERVANT A TRANSFERER LES DONNEES ENTRE UNE PILE DE REGISTRES ET UNE RESSOURCE MEMOIRE

Patent Applicant/Assignee:
IDEA CORPORATION,
ROSS Jonathan K,
COUTANT Cary A,
THOMPSON Carol L,
ZAHIR Achmed R,

Inventor(s):
ROSS Jonathan K,
COUTANT Cary A,
THOMPSON Carol L ,
ZAHIR Achmed R

Patent and Priority Information (Country, Number, Date):
Patent: WO 9917207 A1 19990408
Application: WO 98US20746 19980930 (PCT/WO US9820746)
Priority Application: US 97940834 19970930

Designated States: AL AM AT AT AU AZ BA BB BG BR BY CA CH CN CU CZ CZ DE DE DK DK EE EE ES FI FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

Main International Patent Class: **G06F-012/02**

Publication Language: English

Fulltext Availability:
Detailed Description
Claims

Fulltext Word Count: 4887

English Abstract

A computer-implemented method and apparatus for transferring the

contents of a general register (80), in a register stack (86), to a location in a backing store (94) in a main memory (82). When transferring the contents of a general register to a location in the backing store, the invention proposes collecting attribute bits included in each general register of a predetermined group of registers in a temporary collection register (108 or 110). Once the temporary collection register has been filled, the contents of this register are written to the next available location in the backing store. Similarly, on the restoration of registers from the backing store, a collection of attribute bits saved in the backing register is transferred to a temporary collection register. Thereafter, each attribute bit is saved together with associated data into a general register, thereby to restore the former contents of each general register.

French Abstract

L'invention concerne un procede informatique et un appareil destine a transferer le contenu d'un registre general, dans une pile de registre, vers un emplacement dans une memoire auxiliaire faisant partie de la memoire principale. Selon l'invention, lors du transfert du contenu d'un registre general vers un emplacement dans la memoire auxiliaire, on recueille les bits d'attribut, contenus dans chaque registre general faisant partie d'un groupe predefini de registres, dans un registre de collecte temporaire. Une fois le registre de collecte temporaire rempli, le contenu de ce registre est enregistre a l'emplacement suivant, disponible dans la memoire auxiliaire. D'une facon similaire, lors de la restauration des registres a partir de la memoire auxiliaire, on transfere une collection de bits d'attribution sauvegardee dans la memoire auxiliaire a destination d'un registre de collecte temporaire. Par la suite, chaque bit d'attribut est sauvegarde avec les donnees qui s'y rapportent dans un registre general, ce qui a pour effet de restaurer l'ancien contenu de chaque registre general.

5/5/7 (Item 1 from file: 350)

016135064 **Image available**
WPI Acc No: 2004-292940/200427
XRPX Acc No: N04-232533

Compiler based automated error recovery method for computer application, involves automatically generating executable check point object code for recovery, if execution of program is interrupted

Patent Assignee: HEWLETT-PACKARD DEV CO LP (HEWP)
Inventor: DWYER L D K B; **THOMPSON C L** ; ZIEGLER M L

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6708288	B1	20040316	US 2000702590	A	20001031	200427	B

Priority Applications (No Type Date): US 2000702590 A 20001031
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6708288	B1		10	G06F-011/00	

Abstract (Basic): US 6708288 B1

NOVELTY - Program source code is compiled into intermediate code. Check points identified in the intermediate program code, are associated with data objects. Executable check point code for execution at the check points, is automatically generated in which the check point code is configured to store state information of the associated data objects for recovery, if execution of the program is interrupted.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) error recovery apparatus; and

(2) error recovery program product.

USE - For compilers in computer applications e.g. transaction

processing application.
ADVANTAGE - Enables automatically generating check point object code without having check points specified in the source code, thus reducing the developer's task.
DESCRIPTION OF DRAWING(S) - The figure shows a flowchart explaining automated error recovery method.
pp; 10 DwgNo 1/4
Title Terms: COMPILE; BASED; AUTOMATIC; ERROR; RECOVER; METHOD; COMPUTER; APPLY; AUTOMATIC; GENERATE; EXECUTE; CHECK; POINT; OBJECT; CODE; RECOVER; EXECUTE; PROGRAM; INTERRUPT
Derwent Class: T01
International Patent Class (Main): **G06F-011/00**
File Segment: EPI

5/5/8 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016098534 **Image available**
WPI Acc No: 2004-256410/200424
Related WPI Acc No: 2004-050649
XRPX Acc No: N04-203831
Program code compiling method, involves delineating object code segment sets by checkpoints in program code and generating checkpoint code for execution at checkpoints to save state information of program
Patent Assignee: THOMPSON C L (THOM-I)
Inventor: **THOMPSON C L**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040034814	A1	20040219	US 2000702592	A	20001031	200424 B
			US 2003644619	A	20030820	

Priority Applications (No Type Date): US 2000702592 A 20001031; US 2003644619 A 20030820
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040034814	A1		10	H02H-003/05	Cont of application US 2000702592 Cont of patent US 6658656

Abstract (Basic): US 20040034814 A1
NOVELTY - The method involves generating a set of object code segments optimized at an optimization level. Another set of segments associated with the former set is optimized at another level. Checkpoints in a program code delineate the object code segment sets. Checkpoint code is generated for execution at the checkpoints. The code saves state information of the program.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) an apparatus for compiling program code
(b) an article of manufacture comprising a computer readable medium with instructions for causing a processor to perform program code compiling method.
USE - Used for compiling program code for recovering from fatal errors encountered in executing computer program code.
ADVANTAGE - The method processes the intermediate code on a segment by segment basis, thereby eliminating the step of undoing the optimizations that introduces the errors. The method generates alternative code that supports recovery from a fatal program error.
DESCRIPTION OF DRAWING(S) - The drawing shows a flowchart of an example process for error recovery in accordance with program compilation techniques.
pp; 10 DwgNo 4/4
Title Terms: PROGRAM; CODE; COMPILE; METHOD; DELINEATE; OBJECT; CODE; SEGMENT; SET; CHECKPOINT; PROGRAM; CODE; GENERATE; CHECKPOINT; CODE; EXECUTE; CHECKPOINT; SAVE; STATE; INFORMATION; PROGRAM

Derwent Class: T01
International Patent Class (Main): H02H-003/05
International Patent Class (Additional): **G06F-009/44 ; G06F-009/45 ;** H03K-019/03
File Segment: EPI

5/5/9 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

016098075 **Image available**
WPI Acc No: 2004-255951/200424
XRPX Acc No: N04-203403

Processing system for efficiently processing a program that includes assertion instructions, has compiler enabling selective execution of assertion handling code based on run time input in response to failed assertion test

Patent Assignee: HEWLETT-PACKARD DEV CO LP (HEWP)
Inventor: DWYER L D K B; **THOMPSON C L**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6701518	B1	20040302	US 2000631552	A	20000803	200424	B

Priority Applications (No Type Date): US 2000631552 A 20000803
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6701518	B1		14	G06F-009/44	

Abstract (Basic): US 6701518 B1
NOVELTY - The system has a compiler for translating the first function of a first program stored in a memory into the second function of a second program. The compiler enables selective execution of assertion handling code based on the run time input in response to a failed assertion test defined by the translated assertion instructions.
DETAILED DESCRIPTION - The first function includes assertion instructions, while the second function includes the translated assertion instructions. The compiler enables selective execution of a portion of the translated assertion executions based on the run time input. An INDEPENDENT CLAIM is included for efficiently processing a program that includes assertion instructions.
USE - For enabling selective assertion of testing computer programs based on run time inputs.
ADVANTAGE - Reduces the adverse impact of assertion instructions to processor performance to encourage programmers to include assertion instructions in computer programs.
DESCRIPTION OF DRAWING(S) - The figure is a block diagram showing a function compiled by a compiler in efficiently processing a program.
pp; 14 DwgNo 4/7
Title Terms: PROCESS; SYSTEM; EFFICIENCY; PROCESS; PROGRAM; INSTRUCTION; COMPILE; ENABLE; SELECT; EXECUTE; HANDLE; CODE; BASED; RUN; TIME; INPUT; RESPOND; FAIL; TEST
Derwent Class: T01
International Patent Class (Main): **G06F-009/44**
File Segment: EPI

5/5/10 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015997807 **Image available**
WPI Acc No: 2004-155657/200415
XRPX Acc No: N04-124564

Computer program data structure invariant property verification method involves verifying whether runtime value of data structure is consistent

with invariant property during execution
Patent Assignee: LITTFIN J (LITT-I); THOMPSON C L (THOM-I)
Inventor: **LITTFIN J ; THOMPSON C L**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040015897	A1	20040122	US 2001858241	A	20010515	200415	B

Priority Applications (No Type Date): US 2001858241 A 20010515
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040015897	A1		6	G06F-009/44	

Abstract (Basic): US 20040015897 A1

NOVELTY - A code verifying whether a runtime value of data structure is consistent with invariant property, is automatically generated in response to annotation of data structure in source code. The runtime value is compared to invariant property in the generated code, during execution of program. If the runtime property is inconsistent with the invariant property, the program branches to exception handler code.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for apparatus for verifying invariant property of data structure of computer program at run time.

USE - For verifying invariant property which is range of data values, of data structures of computer programs in variety of programming languages for e.g. C and C++, at runtime.

ADVANTAGE - Avoids the need for a developer to specify the range of valid addresses for code or data, since the compiler determines the valid range of addresses of code or data. Realizes a method capable of being applicable to a variety of programming languages particularly beneficial in compiled languages, for e.g. C and C++.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the process of verifying invariant properties of data structures at runtime.

pp; 6 DwgNo 2/2

Title Terms: COMPUTER; PROGRAM; DATA; STRUCTURE; INVARIANT; PROPERTIES; VERIFICATION; METHOD; VERIFICATION; VALUE; DATA; STRUCTURE; CONSISTENT; INVARIANT; PROPERTIES; EXECUTE
Derwent Class: T01
International Patent Class (Main): **G06F-009/44**
International Patent Class (Additional): **G06F-009/45** ; H02H-003/05
File Segment: EPI

5/5/11 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015949706 **Image available**
WPI Acc No: 2004-107547/200411
XRPX Acc No: N04-085493

Register allocation method in optimizing compiler, involves assigning variables having lifetime greater than initiation interval of source code programming loop, to rotating register
Patent Assignee: SRINIVASAN U (SRIN-I); THOMPSON C (THOM-I)
Inventor: SRINIVASAN U; **THOMPSON C**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030237080	A1	20031225	US 2002177343	A	20020619	200411	B

Priority Applications (No Type Date): US 2002177343 A 20020619
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030237080	A1		19	G06F-009/45	

Abstract (Basic): US 20030237080 A1

NOVELTY - A rotating register is allocated for each identified variables having lifetime greater than initiation interval of a present source code programming loop, when the variables are initiated within the programming loop. A scalar register allocator connected to the rotating register, assigns variables outside of the programming loop, to an allocated and unassigned rotating register.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) computer readable medium storing register allocation program;
(2) compiler; and
(3) optimizing complier.

USE - For allocating register in optimizing compiler (claimed) for microprocessor of computer.

ADVANTAGE - Efficiently improves register allocation in optimizing compiler.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining register allocation method.

pp; 19 DwgNo 9/9

Title Terms: REGISTER; ALLOCATE; METHOD; OPTIMUM; COMPILE; ASSIGN; VARIABLE ; LIFETIME; GREATER; INITIATE; INTERVAL; SOURCE; CODE; PROGRAM; LOOP; ROTATING; REGISTER

Derwent Class: T01

International Patent Class (Main): **G06F-009/45**

International Patent Class (Additional): **G06F-015/00**

File Segment: EPI

5/5/12 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015923564 **Image available**

WPI Acc No: 2004-081404/200408

XRPX Acc No: N04-065087

Code generation method for module scheduled uncounted loops in compilers, involves assigning stage predicate to each instruction in each speculative stage to conditionally enable or disable instruction execution

Patent Assignee: HANK R E (HANK-I); MORRIS D (MORR-I); SRINIVASAN U (SRIN-I); THOMPSON C L (THOM-I)

Inventor: HANK R E; MORRIS D; SRINIVASAN U; **THOMPSON C L**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030233643	A1	20031218	US 2002175375	A	20020618	200408	B

Priority Applications (No Type Date): US 2002175375 A 20020618

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030233643	A1		28	G06F-009/45	

Abstract (Basic): US 20030233643 A1

NOVELTY - A given stage predicate is assigned to each instruction in each speculative stage, and the stage predicate is used to conditionally enable or disable the execution of an instruction during the prologue and epilogue execution.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) counted loops processing method;
(2) fully if-converted loops processing method;
(3) uncounted loops processing method;
(4) module scheduling apparatus; and
(5) computer program product for generating codes for modules scheduled uncounted loops.

USE - For generating codes for module scheduled uncounted loops in compilers in computer system.

ADVANTAGE - By assigning stage predicates to instructions in the speculative stages, unconditional and unnecessary execution of speculative loads and the cost of bringing in unnecessary data into the data cache are avoided.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the scheduler and register allocator.

global and loop optimizer (320)
schedule and register allocator (330)
global scheduler (410)
module scheduler and register assigner (420)

pp; 28 DwgNo 4/10

Title Terms: CODE; GENERATE; METHOD; MODULE; SCHEDULE; LOOP; ASSIGN; STAGE; INSTRUCTION; STAGE; CONDITIONAL; ENABLE; DISABLE; INSTRUCTION; EXECUTE

Derwent Class: T01

International Patent Class (Main): **G06F-009/45**

File Segment: EPI

5/5/13 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015902976 **Image available**

WPI Acc No: 2004-060816/200406

XRPX Acc No: N04-049259

Computer program modification method involves including prefetch instructions prior to instructions corresponding to cache-miss conditions, when frequency of recurring patterns is more than selected frequency

Patent Assignee: HEWLETT-PACKARD CO (HEWP)

Inventor: **THOMPSON C L**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030225996	A1	20031204	US 2002160476	A	20020530	200406	B

Priority Applications (No Type Date): US 2002160476 A 20020530

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030225996	A1		10	G06F-015/00	

Abstract (Basic): US 20030225996 A1

NOVELTY - Profile data including instruction and target addresses, loaded and stored data, and the execution counts, is generated for executed load and store instructions. Recurring patterns of the instructions corresponding to cache-miss conditions, are identified from profile data. Prefetch instructions are included prior to the instructions of the patterns, when recurring frequency is more than selected frequency.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) computer readable storage medium storing computer program modification program; and

(2) apparatus for modifying computer program.

USE - For modifying computer program by including prefetch instructions corresponding to cache-miss patterns.

ADVANTAGE - Since prefetch instructions are included corresponding to the cache-miss condition, waiting time for acquiring stored data from the memory is eliminated. Hence program execution time of the processor, is shortened.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the program modification process.

pp; 10 DwgNo 1/3

Title Terms: COMPUTER; PROGRAM; MODIFIED; METHOD; INSTRUCTION; PRIOR; INSTRUCTION; CORRESPOND; CACHE; MISS; CONDITION; FREQUENCY; RECURRENCE; PATTERN; MORE; SELECT; FREQUENCY

Derwent Class: T01

International Patent Class (Main): **G06F-015/00**
International Patent Class (Additional): **G06F-009/45**
File Segment: EPI

5/5/14 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015892814 **Image available**
WPI Acc No: 2004-050649/200405
Related WPI Acc No: 2004-256410
XRPX Acc No: N04-040913

Program code compiling method, involves creating checkpoint code for execution at checkpoints to save program state information and selecting object code segment for execution in response to program execution error

Patent Assignee: HEWLETT-PACKARD DEV CO LP (HEWP)
Inventor: **THOMPSON C L**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6658656	B1	20031202	US 2000702592	A	20001031	200405	B

Priority Applications (No Type Date): US 2000702592 A 20001031
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6658656	B1		9	G06F-009/45	

Abstract (Basic): US 6658656 B1

NOVELTY - The method involves generating two sets of object code segments optimized at two optimization levels, and identifying checkpoints in a program code during compilation. Checkpoint code is generated for execution at the checkpoints to save state information of the program. One object code segment is selected from among the code segments for execution in response to a program execution error.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) an apparatus for compiling program code

(2) a computer program product to cause a computer to perform program code compilation.

USE - Used for compiling a program code.

ADVANTAGE - The method creates alternative versions of code segments and dynamically substitutes execution of the alternative code versions.

DESCRIPTION OF DRAWING(S) - The drawing shows a flowchart of a process for error recovery based on program compilation.

pp; 9 DwgNo 4/4

Title Terms: PROGRAM; CODE; COMPILE; METHOD; CHECKPOINT; CODE; EXECUTE; CHECKPOINT; SAVE; PROGRAM; STATE; INFORMATION; SELECT; OBJECT; CODE; SEGMENT; EXECUTE; RESPOND; PROGRAM; EXECUTE; ERROR
Derwent Class: T01
International Patent Class (Main): **G06F-009/45**
International Patent Class (Additional): **G06F-009/44**
File Segment: EPI

5/5/15 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015882897 **Image available**
WPI Acc No: 2004-040730/200404
XRPX Acc No: N04-033009

Register access management method for use in microprocessor, involves determining whether register referenced by instruction is within current register stack frame, based on which instruction is executed

Patent Assignee: INST DEV EMERGING ARCHITECTURES LLC (EMER-N)

Inventor: COUTANT C A; ROSS J K; **THOMPSON C L** ; ZAHIR A R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6665793	B1	20031216	US 99473820	A	19991228	200404	B

Priority Applications (No Type Date): US 99473820 A 19991228
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6665793	B1		17	G06F-009/312	

Abstract (Basic): US 6665793 B1

NOVELTY - The method involves determining whether a register referenced by an instruction is in a current register stack frame. The instruction is executed to write data into the register or to read data from the register, when the register is determined to be within the current register stack frame.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) register access management apparatus; and

(2) microprocessor.

USE - For managing access to register used in microprocessor (claimed).

ADVANTAGE - Prevents a program executing on microprocessor from overwriting registers that are in stack frames.

DESCRIPTION OF DRAWING(S) - The figures show the flowchart illustrating the register access management process.

pp; 17 DwgNo 4, 5/6

Title Terms: REGISTER; ACCESS; MANAGEMENT; METHOD; MICROPROCESSOR; DETERMINE; REGISTER; REFERENCE; INSTRUCTION; CURRENT; REGISTER; STACK; FRAME; BASED; INSTRUCTION; EXECUTE
Derwent Class: T01
International Patent Class (Main): **G06F-009/312**
File Segment: EPI

5/5/16 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015834157 **Image available**
WPI Acc No: 2003-896361/200382
XRPX Acc No: N03-715280

Computer program code executing system, has processing circuitry to execute unconditional branch instruction based on mode indicator when code is disabled and refrains from instruction, and executing code when code is enabled

Patent Assignee: HEWLETT-PACKARD DEV CO LP (HEWP)
Inventor: HUCK J; **THOMPSON C L**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6654877	B1	20031125	US 2000644435	A	20000823	200382	B

Priority Applications (No Type Date): US 2000644435 A 20000823
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6654877	B1		10	G06F-009/44	

Abstract (Basic): US 6654877 B1

NOVELTY - The system has a processing circuitry (32) that receives run time data indicating whether a set of codes is enabled or disabled. A value of a mode indicator (71) is set based on the data. The circuitry executes an unconditional branch instruction based on the indicator when the code is disabled and refrains to execute the instruction based on the indicator. The circuitry executes the set of code on enabling.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of selectively executing sets of code in computer programs.

USE - Used for selectively executing sets of code in a computer program.

ADVANTAGE - The presence of the disabled code in the program does not affect the performance of the program since the execution of the code is based on the status of the mode indicator. The circuitry executes unconditional branch instruction based on the mode indicator, thereby preventing execution of the set of code when the code is disabled.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a processing circuitry in a computer system.

Processing circuitry (32)
Mode indicator (71)
Instruction dispersal unit (75)
Control circuitry (77)
Pipelines (79)
pp; 10 DwgNo 3/4

Title Terms: COMPUTER; PROGRAM; CODE; EXECUTE; SYSTEM; PROCESS; CIRCUIT; EXECUTE; UNCONDITIONAL; BRANCH; INSTRUCTION; BASED; MODE; INDICATE; CODE; DISABLE; INSTRUCTION; EXECUTE; CODE; CODE; ENABLE
Derwent Class: T01
International Patent Class (Main): **G06F-009/44**
International Patent Class (Additional): **G06F-009/45** ; **G06F-011/36**
File Segment: EPI

5/5/17 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015766823 **Image available**
WPI Acc No: 2003-829025/200377
XRPX Acc No: N03-662324

Computer system e.g. portable computer system, has processor which selects specific branch instruction identifier based on value of mode indicator so as to branch processing

Patent Assignee: HEWLETT-PACKARD DEV CO LP (HEWP)
Inventor: HUCK J; **THOMPSON C L**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6643769	B1	20031104	US 2000644315	A	20000823	200377	B

Priority Applications (No Type Date): US 2000644315 A 20000823
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6643769	B1		10	G06F-009/32	

Abstract (Basic): US 6643769 B1

NOVELTY - A processor (32) executes the instruction of memory based on the address identifiers included in the branch instructions. A specific identifier is selected based on the value of mode indicator (55) during execution of branch instructions. The processing is branched using the identifiers, in response to the enabling and disabling of codes.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for selective computer code execution method.

USE - Computer system e.g. portable computer system.

ADVANTAGE - Execution of computer code is either enabled or disabled by controlling the value of mode indicator thereby flexible validation is achieved. Flipping operation is performed quickly without delaying the execution of branch instruction thereby quickens validation time.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of computer system.

memory (29)

processor (32)
local interface (36)
input unit (38)
mode indicator (55)
pp; 10 DwgNo 1/3
Title Terms: COMPUTER; SYSTEM; PORTABLE; COMPUTER; SYSTEM; PROCESSOR; SELECT; SPECIFIC; BRANCH; INSTRUCTION; IDENTIFY; BASED; VALUE; MODE; INDICATE; SO; BRANCH; PROCESS
Derwent Class: T01
International Patent Class (Main): **G06F-009/32**
International Patent Class (Additional): **G06F-009/44 ; G06F-011/36**
File Segment: EPI

5/5/18 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015684173 **Image available**
WPI Acc No: 2003-746362/200370
XRPX Acc No: N03-598044

Code characteristic graphic representation providing method involves displaying unique graphical indicator along with block of code in program, to indicate presence of instruction characteristic in block of code

Patent Assignee: COUTANT C A (COUT-I); THOMPSON C L (THOM-I)
Inventor: COUTANT C A; **THOMPSON C L**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030167457	A1	20030904	US 200287407	A	20020301	200370	B

Priority Applications (No Type Date): US 200287407 A 20020301
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030167457	A1		17	G06F-009/44	

Abstract (Basic): US 20030167457 A1

NOVELTY - A block of code in a program, is acquired and analyzed for an instruction characteristic. An unique graphical indicator generated for the instruction characteristic, is displayed along with the block of code to indicate the presence of instruction characteristic in block of code.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) code characteristic graphic representation providing system; and

(2) computer readable medium for storing code characteristic graphic representation.

USE - For producing graphic representations of code characteristic.

ADVANTAGE - Conveys information to a developer/programmer about the characteristics of the optimized code.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart illustrating utilization of optimized code.

pp; 17 DwgNo 4/10
Title Terms: CODE; CHARACTERISTIC; GRAPHIC; REPRESENT; METHOD; DISPLAY; UNIQUE; GRAPHICAL; INDICATE; BLOCK; CODE; PROGRAM; INDICATE; PRESENCE; INSTRUCTION; CHARACTERISTIC; BLOCK; CODE
Derwent Class: T01
International Patent Class (Main): **G06F-009/44**
International Patent Class (Additional): **G06F-009/45**
File Segment: EPI

5/5/19 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015584223 **Image available**
WPI Acc No: 2003-646380/200361
Related WPI Acc No: 2003-627801
XRPX Acc No: N03-514167

Information organizing method for data mining purposes in electronic information systems, comprises providing a visualization of actor communications in the context of one or more discussions

Patent Assignee: CATAPHORA INC (CATA-N)
Inventor: CHARNOCK E B; ROBERTS S L; **THOMPSON C**
Number of Countries: 100 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200367497	A1	20030814	WO 2003US3504	A	20030204	200361	B
AU 2003207856	A1	20030902	AU 2003207856	A	20030204	200425	

Priority Applications (No Type Date): US 2002354403 P 20020204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200367497	A1	E	103	G06F-017/60	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT SD SE SI SK SL SZ TR TZ UG ZM ZW

AU 2003207856 A1 G06F-017/60 Based on patent WO 200367497

Abstract (Basic): WO 200367497 A1

NOVELTY - A method of organizing information comprises providing a visualization of actor (310) communications in the context of one or more electronic paper trails, or discussions (305), where a discussion includes at least one actor and at least one documented communication. A documented communication may be one or more of, a document, an email, an instant message, a facsimile, a voicemail, a phone call, a wire transfer, a fund transfer or an electronically traceable package.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an apparatus to present data.

USE - For data mining purposes in electronic information systems, by visualizing the relationships among and enabling retrieval of one or more groups of documents satisfying a user-defined criterion or set of criteria.

ADVANTAGE - The visualization of actor communications in the context of one or more discussions enables a search technique that can return sets of related documents that are not merely grouped by textual similarity, but also grouped and sequenced according to the social context in which they were created, modified or quoted, thus making it possible to retrieve a very precise set of documents from a large corpus of data using relatively simple search queries.

DESCRIPTION OF DRAWING(S) - The figure is a block diagram of navigation flow in one embodiment of an apparatus to visually present discussions for data mining purposes.

pp; 103 DwgNo 3/40

Title Terms: INFORMATION; ORGANISE; METHOD; DATA; MINE; PURPOSE; ELECTRONIC ; INFORMATION; SYSTEM; COMPRISE; ACTOR; COMMUNICATE; CONTEXT; ONE; MORE
Derwent Class: T01
International Patent Class (Main): **G06F-017/60**
International Patent Class (Additional): **G06F-011/30** ; **G06F-011/300**
File Segment: EPI

5/5/20 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015291587 **Image available**
WPI Acc No: 2003-352520/200333
XRPX Acc No: N03-281555

Team member profile for collaboration among geographically-dispersed team members, stores information defining preferences of members for participating in different types of communication

Patent Assignee: BELL CANADA (BELL-N); NORTEL NETWORKS LTD (NELE)
Inventor: BOUCHARD J J; FORTIER S F; GROSSNER C P; ROMANIUK R; **THOMPSON C** ; WILLIAMS L L
Number of Countries: 099 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020078150	A1	20020620	US 2000738292	A	20001218	200333	B
WO 200250721	A2	20020627	WO 2001CA1740	A	20011207	200333	
AU 200215731	A	20020701	AU 200215731	A	20011207	200333	
CA 2358363	A1	20020618	CA 2358363	A	20011005	200333	

Priority Applications (No Type Date): US 2000738292 A 20001218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020078150	A1		71	G06F-015/16	
WO 200250721	A2	E		G06F-017/60	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

AU 200215731	A		G06F-017/60	Based on patent WO 200250721
CA 2358363	A1	E	H04L-029/10	

Abstract (Basic): US 20020078150 A1

NOVELTY - The team member profile comprises communication information defining the preferences of the respective team members for participating in each of the different types of communication.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for method of enabling a team member to select a profile.

USE - For collaborating among geographically-dispersed team members using a distributed application.

ADVANTAGE - Enables automatically using the communication preferences of the users to control the setup of the communication sessions in which the user is participant.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the collaboration service implementing system.

pp; 71 DwgNo 2/36

Title Terms: TEAM; MEMBER; PROFILE; GEOGRAPHICAL; DISPERSE; TEAM; MEMBER; STORAGE; INFORMATION; DEFINE; MEMBER; PARTICIPATING; TYPE; COMMUNICATE
Derwent Class: T01
International Patent Class (Main): **G06F-015/16 ; G06F-017/60 ;** H04L-029/10
International Patent Class (Additional): H04L-012/16; H04M-003/42
File Segment: EPI

5/5/21 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015270642 **Image available**
WPI Acc No: 2003-331571/200331
XRPX Acc No: N03-265664

Data prefetch apparatus for computer system, prefetches data associated with critical memory references indicating prefetch regions in memory, before switched context is resumed

Patent Assignee: DWYER L D K B (DWYE-I); HUCK J C (HUCK-I); THOMPSON C L (THOM-I); ZIEGLER M L (ZIEG-I)

Inventor: DWYER L D K B; HUCK J C; **THOMPSON C L** ; ZIEGLER M L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030023663	A1	20030130	US 2001917535	A	20010727	200331	B

Priority Applications (No Type Date): US 2001917535 A 20010727
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030023663	A1		9	G06F-009/00	

Abstract (Basic): US 20030023663 A1

NOVELTY - The apparatus identifies prefetch regions in a memory and corresponding critical memory references, during compilation of a computer program. The references correspond to data needed in a cache memory, if a context switch occurs from a process or thread of one context to another. The data associated with the critical memory references, are prefetched and stored before the switched context is resumed.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for data prefetch method.

USE - For enabling compiler to prefetch data for storage in cache memory, during context switch in computer system.

ADVANTAGE - Since the data is prefetched and stored in the cache memory prior to resuming from the context switch, the data is ready to be referenced efficiently when the thread or process resumes. Therefore, omission of cache data is prevented and bandwidth of the computer system is efficiently utilized.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart illustrating the data prefetch method in the event of context switch.

pp; 9 DwgNo 3A/3

Title Terms: DATA; APPARATUS; COMPUTER; SYSTEM; DATA; ASSOCIATE; CRITICAL; MEMORY; REFERENCE; INDICATE; REGION; MEMORY; SWITCH; CONTEXT; RESUME
Derwent Class: T01
International Patent Class (Main): **G06F-009/00**
File Segment: EPI

5/5/22 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015020647 **Image available**
WPI Acc No: 2003-081164/200308
XRPX Acc No: N03-063508

Static single substitution function implementation method involves materializing static single substitution function, by inserting copy of each source operand related to specific function in target variable

Patent Assignee: HEWLETT-PACKARD CO (HEWP); BALA V (BALA-I); JU D (JUDD-I); SANTHANAM V (SANT-I); THOMPSON C L (THOM-I)
Inventor: BALA V; JU D; SANTHANAM V; **THOMPSON C L**
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002297399	A	20021011	JP 200218235	A	20020128	200308	B
US 20040015919	A1	20040122	US 2001814511	A	20010322	200407	

Priority Applications (No Type Date): US 2001814511 A 20010322
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002297399	A		11	G06F-009/45	
US 20040015919	A1			G06F-009/45	

Abstract (Basic): JP 2002297399 A

NOVELTY - A guard expression is introduced into each source operand with respect to a control command or a function (phip) in a specific order. A copy of each source operand is inserted in a target variable in the same order, to materialize the static single substitution (SSA)

function (phi). Each copy is described by the guard expression with the order related to source operand.

USE - For conversion technique of common sequence of computer.

ADVANTAGE - Performs the static single substitution easily in a short duration using a code with the specific function.

DESCRIPTION OF DRAWING(S) - The figure shows the source code and its control flow diagrammatic chart.

pp; 11 DwgNo 5/8

Title Terms: STATIC; SINGLE; SUBSTITUTE; FUNCTION; IMPLEMENT; METHOD; STATIC; SINGLE; SUBSTITUTE; FUNCTION; INSERT; COPY; SOURCE; OPERAND; RELATED; SPECIFIC; FUNCTION; TARGET; VARIABLE

Derwent Class: T01

International Patent Class (Main): **G06F-009/45**

File Segment: EPI

5/5/23 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014796567 **Image available**

WPI Acc No: 2002-617273/200266

XRPX Acc No: N02-488476

Virtual communication session initiation method for hotline, helpline services, involves selecting communication media corresponding to invitation request, using prestored dynamic presence and availability information of objective person

Patent Assignee: BELL CANADA (BELL-N); NORTEL NETWORKS LTD (NELE)

Inventor: BEATON B F; BOUCHARD J J; FORTIER S F; GROSSNER C P; LIVERSIDGE D E; MERCIER D; ROMANIUK R; SMITH C D R; **THOMPSON C** ; WILLIAMS L L; ZDRALEK J F

Number of Countries: 099 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020076025	A1	20020620	US 2000737958	A	20001218	200266	B
CA 2358353	A1	20020618	CA 2358353	A	20011005	200266	
WO 200250723	A2	20020627	WO 2001CA1749	A	20011207	200266	
AU 200215738	A	20020701	AU 200215738	A	20011207	200269	

Priority Applications (No Type Date): US 2000737958 A 20001218

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020076025	A1		72	H04M-003/42	
CA 2358353	A1	E		H04L-029/10	
WO 200250723	A2	E		G06F-017/60	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

AU 200215738	A		G06F-017/60	Based on patent WO 200250723

Abstract (Basic): US 20020076025 A1

NOVELTY - A request message for inviting a specific person to join a communication session, is sent from the user (4a-4d) to a collaboration service suite (2). The suite determines suitable communication media for the objective person, based on restored dynamic presence and availability information of the person, and transmits the request to the person using the selected media.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for virtual communication session invitation system.

USE - For inviting a person to join a virtual communication session for applications such as customer relation management, in a institutional information exchange, distributed health care administration, hotline and help line services, and other business, political academic applications through wireless telephone, personal

digital assistant (PDA), 2-way payer, PC, telephone of the person.
ADVANTAGE - Provides a user friendly invitation mechanism, by automatically selecting communication media for the purpose.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of interaction between a collaboration services and members.
Collaboration service suite (2)
Users (4a-4d)
pp; 72 DwgNo 1/36
Title Terms: VIRTUAL; COMMUNICATE; SESSION; INITIATE; METHOD; SERVICE; SELECT; COMMUNICATE; MEDIUM; CORRESPOND; REQUEST; DYNAMIC; PRESENCE; AVAILABLE; INFORMATION; OBJECTIVE; PERSON
Derwent Class: T01; W01; W05
International Patent Class (Main): **G06F-017/60** ; H04L-029/10; H04M-003/42
International Patent Class (Additional): **G06F-015/16** ; H04L-012/16
File Segment: EPI

5/5/24 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014786618 **Image available**
WPI Acc No: 2002-607324/200265
XRPX Acc No: N02-480920
Communication initiation method e.g. for multimedia communication, involves enabling person to interact with virtual team environment to select one of person identifier and one of different communication types
Patent Assignee: BELL CANADA (BELL-N); NORTEL NETWORKS LTD (NELE); BEATON B F (BEAT-I); BOUCHARD J J (BOUC-I); FORTIER S F (FORT-I); GROSSNER C P (GROS-I); LIVERSIDGE D E (LIVE-I); ROMANIUK R (ROMA-I); SMITH C D R (SMIT-I); THOMPSON C (THOM-I); WILLIAMS L L (WILL-I); ZDRALEK J F (ZDRA-I)
Inventor: BEATON B F; BOUCHARD J J; FORTIER S F; GROSSNER C P; LIVERSIDGE D E; ROMANIUK R; SMITH C D R; **THOMPSON C** ; WILLIAMS L L; ZDRALEK J F
Number of Countries: 099 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020075306	A1	20020620	US 2000738294	A	20001218	200265	B
CA 2358343	A1	20020618	CA 2358343	A	20011005	200265	
WO 200250725	A2	20020627	WO 2001CA1751	A	20011207	200265	
AU 200215740	A	20020701	AU 200215740	A	20011207	200269	

Priority Applications (No Type Date): US 2000738294 A 20001218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020075306	A1		50	G06F-013/00	
CA 2358343	A1	E		H04L-029/10	
WO 200250725	A2	E		G06F-017/60	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

AU 200215740	A		G06F-017/60	Based on patent WO 200250725

Abstract (Basic): US 20020075306 A1
NOVELTY - A person is enabled to interact with a virtual team environment, by a graphical interface to select one of the different communication types and one of the personal identifiers. The communication session is initiated using the selected communication type and personal identifier.
USE - For initiating communication including one-way messaging, two-way messaging, voice, multimedia, video conferencing, etc.
ADVANTAGE - Flexibility of virtual team environment (VTE) provides power tool to facilitate communications collaboration.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram schematically illustrating communication between the person and the

VTE.
pp; 50 DwgNo 1/36
Title Terms: COMMUNICATE; INITIATE; METHOD; COMMUNICATE; ENABLE; PERSON; INTERACT; VIRTUAL; TEAM; ENVIRONMENT; SELECT; ONE; PERSON; IDENTIFY; ONE; COMMUNICATE; TYPE
Derwent Class: T01
International Patent Class (Main): **G06F-013/00 ; G06F-017/60 ;** H04L-029/10
International Patent Class (Additional): H04L-012/16
File Segment: EPI

5/5/25 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014777902 **Image available**
WPI Acc No: 2002-598608/200264
XRPX Acc No: N02-474762

Graphical user interface for virtual team environment, accesses and displays preference and presence information relating to each member of team maintained by collaborative service suite based on request from one team member

Patent Assignee: BELL CANADA (BELL-N); NORTEL NETWORKS LTD (NELE); BEATON B F (BEAT-I); BOUCHARD J J (BOUC-I); FORTIER S F (FORT-I); GROSSNER C P (GROS-I); LIVERSIDGE D E (LIVE-I); ROMANIUK R (ROMA-I); SMITH C D R (SMIT-I); THOMPSON C (THOM-I); WILLIAMS L L (WILL-I); ZDRALEK J F (ZDRA-I)
Inventor: BEATON B F; BOUCHARD J J; FORTIER S F; GROSSNER C P; LIVERSIDGE D E; ROMANIUK R; SMITH C D R; **THOMPSON C** ; WILLIAMS L L; ZDRALEK J F
Number of Countries: 099 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020075305	A1	20020620	US 2000738329	A	20001218	200264	B
WO 200250659	A2	20020627	WO 2001CA1743	A	20011207	200264	
AU 200215733	A	20020701	AU 200215733	A	20011207	200264	
CA 2358393	A1	20020618	CA 2358393	A	20011005	200264	

Priority Applications (No Type Date): US 2000738329 A 20001218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020075305	A1		48	G06F-013/00	
WO 200250659	A2	E		G06F-009/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

AU 200215733	A		G06F-009/00	Based on patent WO 200250659
CA 2358393	A1	E	H04L-029/10	

Abstract (Basic): US 20020075305 A1

NOVELTY - The virtual team environment (VTE) client accesses and displays the preference and presence information relating to each member of the team maintained by the collaborative services suite (2) in response to request from one team member. The VTE client initiates specific type of communication selected by one team member, with other member.

USE - For virtual team environment.

ADVANTAGE - Provides user friendly, intuitive mechanism that facilitates collaboration among member of geographically dispersed team, graphical user interface displays dynamic preference and presence information for each member of the team, so that the user has awareness of each of the other team members.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of interactions between collaboration service suite and team members.

Collaboration service suite (2)
pp; 48 DwgNo 1/36
Title Terms: GRAPHICAL; USER; INTERFACE; VIRTUAL; TEAM; ENVIRONMENT; ACCESS ; DISPLAY; PREFER; PRESENCE; INFORMATION; RELATED; MEMBER; TEAM; MAINTAIN ; SERVICE; SUITE; BASED; REQUEST; ONE; TEAM; MEMBER
Derwent Class: T01
International Patent Class (Main): **G06F-009/00** ; **G06F-013/00** ; H04L-029/10
International Patent Class (Additional): **G06F-017/60** ; H04L-012/16
File Segment: EPI

5/5/26 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014777901 **Image available**
WPI Acc No: 2002-598607/200264
XRPX Acc No: N02-474761

Communication facilitating distribution application for geographically dispersed team members, has interface to display dynamic availability information of team members to allow team member to initiate communication

Patent Assignee: BELL CANADA (BELL-N); NORTEL NETWORKS LTD (NELE)
Inventor: BEATON B F; BOUCHARD J J; FORTIER S F; GROSSNER C P; LIVERSIDGE D E; MERCIER D; ROMANIUK R; SMITH C D R; **THOMPSON C** ; WILLIAMS L L; ZDRALEK J F
Number of Countries: 099 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020075304	A1	20020620	US 2000738293	A	20001218	200264	B
WO 200250722	A2	20020627	WO 2001CA1741	A	20011207	200264	
AU 200215732	A	20020701	AU 200215732	A	20011207	200264	
CA 2358328	A1	20020618	CA 2358328	A	20011005	200264	

Priority Applications (No Type Date): US 2000738293 A 20001218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020075304	A1		75	G06F-013/00	
WO 200250722	A2	E		G06F-017/60	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

AU 200215732	A		G06F-017/60	Based on patent WO 200250722
CA 2358328	A1	E	H04L-012/18	

Abstract (Basic): US 20020075304 A1

NOVELTY - An interface displays dynamic presence and availability information and allows a team member to request for initiating a communication session with another team member to a collaboration services suite. A collaboration services suite application (2) establishes a communication session between several team members using a communication media in response to the request from the team member.

USE - Distributed application for facilitating collaboration between geographically dispersed team members for business, academic, political or other social reasons. Also for applications such as customer relation management, institutional information exchange, distributed healthcare administration, hot-line and help-line services. For communicating using wireless personal digital assistant (PDA), wireless telephone, two-way pager device, personal computer.

ADVANTAGE - A user-friendly, intuitive mechanism is provided that facilitates seamless two-party and multiparty communication among members of a geographically dispersed team, without the user requiring to have prior knowledge of network addresses or communication setup

procedures.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram schematically illustrating interactions between the collaboration services suite and team members.

Collaboration services suite application (2)

pp; 75 DwgNo 1/36

Title Terms: COMMUNICATE; FACILITATE; DISTRIBUTE; APPLY; GEOGRAPHICAL; DISPERSE; TEAM; MEMBER; INTERFACE; DISPLAY; DYNAMIC; AVAILABLE; INFORMATION; TEAM; MEMBER; ALLOW; TEAM; MEMBER; INITIATE; COMMUNICATE

Derwent Class: T01; W01

International Patent Class (Main): **G06F-013/00 ; G06F-017/60 ;** H04L-012/18

International Patent Class (Additional): H04L-012/16; H04M-003/56

File Segment: EPI

5/5/27 (Item 21 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014762360 **Image available**

WPI Acc No: 2002-583064/200262

XRPX Acc No: N02-462428

Knowledge management system for document related service and recommender service, records requested item and generates cover sheet including knowledge management service of requested item in response to user request

Patent Assignee: XEROX CORP (XERO)

Inventor: GRASSO A; MEUNIER J; **THOMPSON C**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020080387	A1	20020627	US 2000746913	A	20001222	200262	B

Priority Applications (No Type Date): US 2000746913 A 20001222

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020080387	A1		11	G06F-015/00	

Abstract (Basic): US 20020080387 A1

NOVELTY - A printer (10) in response to an user request, records a requested item on a paper. For each item requested to be recorded, the printer generates a cover sheet (20) containing human readable marks to identify requesting user, the item recorded and a knowledge management service (12) associated with the requested item. The service (12) stores a record of user request with an electronic version of requested item in a repository (60).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Information management method;

(2) Recommendation generation method; and

(3) Cover sheet.

USE - Knowledge management system employing paper user interface system e.g. Xerox flowport system for providing document related services and recommender services.

ADVANTAGE - Provides a cover sheet which becomes an input, output and surrogate document mechanism enabling access to both document repositories and associated knowledge management services easily which enables the users to rate their printed document to hold a quantitative measure of its value.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the knowledge management system.

Printer (10)

Knowledge management service (12)

Cover sheet (20)

Repository (60)

pp; 11 DwgNo 1/4

Title Terms: MANAGEMENT; SYSTEM; DOCUMENT; RELATED; SERVICE; SERVICE; RECORD; REQUEST; ITEM; GENERATE; COVER; SHEET; MANAGEMENT; SERVICE; REQUEST; ITEM; RESPOND; USER; REQUEST
Derwent Class: T01; T04
International Patent Class (Main): **G06F-015/00**
International Patent Class (Additional): G06K-001/00
File Segment: EPI

5/5/28 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014762146 **Image available**
WPI Acc No: 2002-582850/200262
XRPX Acc No: N02-462231

Virtual team environment establishing system for collaborating geographically dispersed team members, initiates request for communication session with team member by selecting associated communications icon

Patent Assignee: BELL CANADA (BELL-N); NORTEL NETWORKS LTD (NELE)
Inventor: BEATON B F; BOUCHARD J J; FORTIER S F; GROSSNER C P; LIVERSIDGE D E; MERCIER D; ROMANIUK R; SMITH C D R; **THOMPSON C** ; WILLIAMS L L; ZDRALEK J F
Number of Countries: 099 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020075303	A1	20020620	US 2000737957	A	20001218	200262	B
CA 2358345	A1	20020618	CA 2358345	A	20011005	200262	
WO 200250724	A2	20020627	WO 2001CA1750	A	20011207	200262	
AU 200215739	A	20020701	AU 200215739	A	20011207	200264	

Priority Applications (No Type Date): US 2000737957 A 20001218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020075303	A1		72	G06F-013/00	
CA 2358345	A1	E		H04L-029/10	
WO 200250724	A2	E		G06F-017/60	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

AU 200215739	A		G06F-017/60	Based on patent WO 200250724

Abstract (Basic): US 20020075303 A1

NOVELTY - A collaboration services suite (2) enables communications between the members of a team using different communications media. A GUI enables team member to view communication icons showing presence and availability data of different communication devices associated with the respective team members and initiates a request for communication session with another member of the team by selecting one of icons associated with other member.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for virtual team environment establishing method.

USE - For facilitating collaboration among geographically dispersed team members.

ADVANTAGE - Provides dynamic preference and round-the-clock presence information to permit transparent communication sessions among team members. The integration of text, voice and multi-media communications facilitated in a single, seamless virtual team environment provides a powerful tool to facilitate collaboration in a manner that closely simulated physical collocation of team members.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram illustrating the interactions between the collaboration services suite and members of a team.

Collaboration services suite (2)
pp; 72 DwgNo 1/36
Title Terms: VIRTUAL; TEAM; ENVIRONMENT; ESTABLISH; SYSTEM; GEOGRAPHICAL; DISPERSE; TEAM; MEMBER; INITIATE; REQUEST; COMMUNICATE; SESSION; TEAM; MEMBER; SELECT; ASSOCIATE; COMMUNICATE
Derwent Class: T01; W01
International Patent Class (Main): **G06F-013/00 ; G06F-017/60 ;** H04L-029/10
International Patent Class (Additional): **G06F-003/00 ;** H04L-012/16
File Segment: EPI

5/5/29 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014687336 **Image available**
WPI Acc No: 2002-508040/200254
XRPX Acc No: N02-402050

Complex object synthesizing method using distributed computing for enterprise application system, involves creating instances for complex object and initiating with test data to load test complex object

Patent Assignee: EMPIRIX INC (EMPI-N); FRIEDMAN G E (FRIE-I); GLIK M V (GLIK-I); MAKAR-LIMANOV S (MAKA-I); THOMPSON C (THOM-I)
Inventor: FRIEDMAN G E; GLIK M V; MAKAR-LIMANOV S; **THOMPSON C**
Number of Countries: 097 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200235357	A2	20020502	WO 2001US45546	A	20011025	200254	B
US 20020053043	A1	20020502	US 2000243944	P	20001027	200254	
			US 2001873605	A	20010604		
AU 200227130	A	20020506	AU 200227130	A	20011025	200257	
US 20040078684	A1	20040422	US 2000243944	P	20001027	200428	
			US 2001873605	A	20010604		
			US 2001947932	A	20010906		

Priority Applications (No Type Date): US 2001947932 A 20010906; US 2000243944 P 20001027; US 2001873605 A 20010604
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200235357	A2	E	41	G06F-011/34	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

US 20020053043 A1	G06F-011/00	Provisional application US 2000243944	
AU 200227130 A	G06F-011/34	Based on patent WO 200235357	
US 20040078684 A1	G06F-011/00	Provisional application US 2000243944	
		CIP of application US 2001873605	

Abstract (Basic): WO 200235357 A2

NOVELTY - A complex object is reflected to determine fields associated with complex object. The Java serialization is used to serialize the complex object to allocate memory space for the object. The instances of the test object are created and initialized with the test data to load test the complex object.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Enterprise test system;
(2) Enterprise system testing method; and
(3) Computer program product for testing an enterprise system.

USE - For synthesizing complex objects using distributed computing for enterprise application system.

ADVANTAGE - The need for code compilation when generating test data for component under test, is eliminated by utilizing Java reflection. Simplifies testing of enterprise systems by setting the context for component under test. The test object can be load tested with user provided data, without the need to invoke the method to construct the object.

DESCRIPTION OF DRAWING(S) - The figure shows the top level block diagram of system testing enterprise system.

pp; 41 DwgNo 1/13

Title Terms: COMPLEX; OBJECT; SYNTHESIS; METHOD; DISTRIBUTE; COMPUTATION; APPLY; SYSTEM; INSTANCE; COMPLEX; OBJECT; INITIATE; TEST; DATA; LOAD; TEST; COMPLEX; OBJECT

Derwent Class: T01

International Patent Class (Main): **G06F-011/00 ; G06F-011/34**

File Segment: EPI

5/5/30 (Item 24 from file: 350)

014686184 **Image available**

WPI Acc No: 2002-506888/200254

XRPX Acc No: N02-401059

Information provision in e-mail glosser, involves using ranked translation choices to produce a choice sequence for whole multitoken expression to present information about sequence to user in understandable language

Patent Assignee: XEROX CORP (XERO)

Inventor: CHANOD J; SEGOND F; **THOMPSON C**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6393389	B1	20020521	US 99401682	A	19990923	200254	B

Priority Applications (No Type Date): US 99401682 A 19990923

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6393389	B1		26	G06F-017/28	

Abstract (Basic): US 6393389 B1

NOVELTY - A subexpression of a multitoken expression in a natural language is received and a choice is obtained for translation of asset of subexpression to another language. A subset of the subexpressions translation choices are ranked and the ranked choices are used to produce a translation choice sequence. The information about the sequence indicating the meaning of the multitoken expression is presented to the user in an understandable language.

DETAILED DESCRIPTION - Glossing is a machine automated translation that can include multiple translations and ambiguities

INDEPENDENT CLAIMS are included for:

(1) Information providing machine;

(2) Article of manufacture comprising recorded medium storing information providing program;

(3) Data transfer method.

USE - For providing information about meaning of multitoken expression in understandable language in glossing web browser, e-mail glosser, news glosser, subtitle glosser and speech translator.

ADVANTAGE - The complexity for appropriately indicating the chosen translations of subexpressions are eliminated by ranking the subexpression translation choices to produce a sequence of translation choices. An entire multitoken expression is handled rather than a single word to form a sequence of translation choices which indicates the meaning of the expression.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic flow diagram for obtaining a sequence of translation choices for a multitoken expression and presenting the information indicating the

meaning of the expression in an understandable language.
pp; 26 DwgNo 1/7
Title Terms: INFORMATION; PROVISION; MAIL; RANK; TRANSLATION; CHOICE; PRODUCE; CHOICE; SEQUENCE; WHOLE; EXPRESS; PRESENT; INFORMATION; SEQUENCE; USER; LANGUAGE
Derwent Class: T01
International Patent Class (Main): **G06F-017/28**
File Segment: EPI

5/5/31 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014178172 **Image available**
WPI Acc No: 2001-662400/200176
Related WPI Acc No: 1999-277123; 2000-654935
XRPX Acc No: N01-493479

Data transfer in microprocessor, involves transferring data portions in on-chip register to off-chip memory resource and to successive collection registers

Patent Assignee: INTEL CORP (ITLC)
Inventor: COUTANT C A; ROSS J R; **THOMPSON C L** ; ZAHIR A R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6314513	B1	20011106	US 97940834	A	19970930	200176	B
			US 9864091	A	19980421		
			US 98199003	A	19981123		

Priority Applications (No Type Date): US 98199003 A 19981123; US 97940834 A 19970930; US 9864091 A 19980421
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6314513	B1		34	G06F-013/00	CIP of application US 97940834 CIP of application US 9864091 CIP of patent US 6065114

Abstract (Basic): US 6314513 B1

NOVELTY - The data portions stored in an on-chip register (106) is transferred to a off-chip memory resource (122) and to a collection register. If the collection register contains a predetermined quantity of stored data, the stored data is transferred to next collection register.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Content restoring method from a memory resource to a register;

(b) Content transferring apparatus between register stack and a memory resource;

(c) Processor;

(d) Computer system

USE - Used in microprocessor for transferring data between a register stack and a memory resource and also in digital signal processors, graphic and video processors or network processors.

ADVANTAGE - The data are easily and efficiently transferred between a register stack and a backing store in the memory resource.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of a microprocessor that incorporates a register stack.

On-chip register (106)

Off-chip memory resource (122)

pp; 34 DwgNo 1/17
Title Terms: DATA; TRANSFER; MICROPROCESSOR; TRANSFER; DATA; PORTION; CHIP; REGISTER; CHIP; MEMORY; RESOURCE; SUCCESSION; COLLECT; REGISTER
Derwent Class: T01
International Patent Class (Main): **G06F-013/00**
File Segment: EPI

5/5/32 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014095072 **Image available**
WPI Acc No: 2001-579286/200165
XRPX Acc No: N01-431136

Customizable electronic invoice system for use on a data processing server-client network with optional security and sender only access to grant authority to modify invoice fields

Patent Assignee: DALEEN TECHNOLOGIES INC (DALE-N)
Inventor: **THOMPSON C** ; YEHIA R; YIN J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6282552	B1	20010828	US 9832529	A	19980227	200165	B

Priority Applications (No Type Date): US 9832529 A 19980227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6282552	B1		10	G06F-017/24	

Abstract (Basic): US 6282552 B1

NOVELTY - Customizable electronic invoice system with optional security and a number of rules for use on a data processing server-client network comprises a document generator (210) connected to a number of clients where one or more senders only have the ability to alter the user invoice (217) fields or define access for client/users to the original document. Also provides tracking of any changes made by recipients to client preferred files.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the methods used by the data processing system for client and server use.

USE - The system is used to provide a customizable electronic invoicing service over a client-server network.

ADVANTAGE - The system provides a method for users and senders to view both the original document and any subsequent changes made before receipt and the ability to authenticate any signatures included with the modifications.

DESCRIPTION OF DRAWING(S) - The drawing shows a functional block diagram of components for the billing processing system.

Bill/Document generator (210)
Original user bill/document (217)
pp; 10 DwgNo 2/5

Title Terms: ELECTRONIC; INVOICING; SYSTEM; DATA; PROCESS; SERVE; CLIENT; NETWORK; OPTION; SECURE; SEND; ACCESS; AUTHORISE; MODIFIED; INVOICING; FIELD
Derwent Class: T01
International Patent Class (Main): **G06F-017/24**
File Segment: EPI

5/5/33 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013844242 **Image available**
WPI Acc No: 2001-328455/200134
Related WPI Acc No: 2001-328447; 2001-328454; 2001-432452
XRPX Acc No: N01-236370

Web-site end-user assessment system for analyzing moods of end-users of web-sites relative to task graphs of web-sites, in which problems associated with end-user moods are fed back to business knowledge users of web-site

Patent Assignee: TROBA INC (TROB-N)
Inventor: BURNS J; CHANG P; CHARNOCK E B; DER QUAELER L; GUZY M H; HERTSCHUH F G N; MAO W; **THOMPSON C**

Number of Countries: 093 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200127850	A2	20010419	WO 2000US28570	A	20001013	200134	B
AU 200112065	A	20010423	AU 200112065	A	20001013	200147	

Priority Applications (No Type Date): US 2000201183 P 20000502; US 99159226 P 19991013
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200127850	A2	E	70	G06F-017/60	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW

AU 200112065	A		G06F-017/60	Based on patent WO 200127850

Abstract (Basic): WO 200127850 A2

NOVELTY - Task models and graphs for a web-site are constructed and various data collectors collect data regarding end-user behavior on the web-site. The data is then sorted and filtered, and information obtained regarding end-user success on the various tasks that can be performed using the different pages on the web-site. Using this information, the task model of the web-site may be augmented with new edges which reflect unexpected end-user path segments.

DETAILED DESCRIPTION - The system for assessing a state of an end-user of a web-site includes a data collector for collecting data regarding the behavior or an end-user on the web-site, and a task model creator for creating a task model and a task graph for a number of tasks on the web-site. A weighting mechanism weighs the data collected by the data collector. A heuristics determination mechanism assesses the state of the end-user, based upon the data collected by the data collector and the weights assigned to the data by the weighting mechanism. INDEPENDENT CLAIMS are included for; a method for assessing a state of an end-user of a web-site; a method for assessing a satisfaction level of an end-user web site.

USE - Analyzing and interpreting customer behavior at e-commerce or other goal orientated web-sites.

ADVANTAGE - Enables determination of mood states of end-users.

DESCRIPTION OF DRAWING(S) - The drawing shows a system in accordance with the invention.

Task model creator (110)
Data collector (120)
Weighter (130)
Heuristics determinator (140)
Report generator (150)

pp; 70 DwgNo 1/8

Title Terms: WEB; SITE; END; USER; ASSESS; SYSTEM; MOOD; END; USER; WEB; SITE; RELATIVE; TASK; GRAPH; WEB; SITE; PROBLEM; ASSOCIATE; END; USER; MOOD; FEED; BACK; BUSINESS; USER; WEB; SITE
Derwent Class: T01; T05
International Patent Class (Main): **G06F-017/60**
File Segment: EPI

5/5/34 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013844234
WPI Acc No: 2001-328447/200134
Related WPI Acc No: 2001-328454; 2001-328455; 2001-432452
XRPX Acc No: N01-236362

Method of displaying customer states at a Website for analyzing customer behavior by displaying graphical representations of tasks performed by

customers and of the movement of customers between tasks
Patent Assignee: TROBA INC (TROB-N)
Inventor: CHARNOCK E B; DER QUAELER L; LIN M Y; **THOMPSON C**
Number of Countries: 093 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200127801	A2	20010419	WO 2000US28476	A	20001013	200134	B
AU 200114326	A	20010423	AU 200114326	A	20001013	200147	

Priority Applications (No Type Date): US 2000201183 P 20000502; US 99159226 P 19991013
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200127801	A2	E	85	G06F-017/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW

AU 200114326	A		G06F-017/00	Based on patent WO 200127801

Abstract (Basic): WO 200127801 A2
NOVELTY - A high level graphical representation of a website may be presented as a campus of buildings each building corresponding to a given task performed by customers on the website. A floor plan view of each task represents the steps of the task as rooms within the building. Certain tasks can be divided into sub-tasks which are represented as multiple floors within the building. Customers are represented graphically within the rooms in the buildings, and may be represented by the location, mood and actions of animated characters.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a system for displaying customer states at a website.
USE - In analyzing customer behavior at a website.
ADVANTAGE - Provides an easy and understandable way of presenting customer states.
pp; 85 DwgNo 0/16
Title Terms: METHOD; DISPLAY; CUSTOMER; STATE; CUSTOMER; DISPLAY; GRAPHICAL ; REPRESENT; TASK; PERFORMANCE; CUSTOMER; MOVEMENT; CUSTOMER; TASK
Derwent Class: T01
International Patent Class (Main): **G06F-017/00**
File Segment: EPI

5/5/35 (Item 29 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013482992 **Image available**
WPI Acc No: 2000-654935/200063
Related WPI Acc No: 1999-277123; 2001-662400
XRPX Acc No: N00-485355
Computer-implemented method of switching contexts in microprocessor, by copying contents of second register to first register if interrupt handler needs to access register stack
Patent Assignee: IDEA CORP (IDEA-N)
Inventor: COUTANT C; RAJE P; ROSS J K; SAXENA S; **THOMPSON C** ; ZAHIR A R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6065114	A	20000516	US 9864091	A	19980421	200063	B

Priority Applications (No Type Date): US 9864091 A 19980421
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6065114	A		23	G06F-009/48	

Abstract (Basic): US 6065114 A

NOVELTY - The occurrence of an interrupt command is determined. A first register (IFM) configured to store a content of a second register (CFM) that is configured to store control information related to a first portion of a register stack of the microprocessor is invalidated. The necessity for an interrupt handler to access the register stack is determined.

DETAILED DESCRIPTION - If the interrupt handler needs to access the register stack, the first register is validated, the content of the second register is copied to the first register, and the register stack engine of the processor is made to exchange information between the first and second portions of the register stack. An INDEPENDENT CLAIM is also included for an execution method of a cover instruction to synchronize an interrupt handler with a register stack engine.

USE - For switching contexts in processor with register stack.

ADVANTAGE - Uses excess processor memory bandwidth to dynamically spill or fill registers from stacked register file to a backing store in a memory concurrently with program execution. Provides a way of synchronizing spilling and filling of registers with a processor's execution of instructions when a switch from a source to a target context is required to make possible a return to the same context and resume operation in the source context as if no context switch occurred. Provides way of saving and restoring, in an efficient manner, the contents of stacked registers of the stacked register file upon interrupt and return from interrupt, respectively.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of a microprocessor in which the computer-implemented method of switching contexts is applied.

pp; 23 DwgNo 5/12

Title Terms: COMPUTER; IMPLEMENT; METHOD; SWITCH; CONTEXT; MICROPROCESSOR; COPY; CONTENT; SECOND; REGISTER; FIRST; REGISTER; INTERRUPT; HANDLE; NEED; ACCESS; REGISTER; STACK

Derwent Class: T01

International Patent Class (Main): **G06F-009/48**

File Segment: EPI

5/5/36 (Item 30 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013351634 **Image available**

WPI Acc No: 2000-523573/200047

XRPX Acc No: N00-386973

Adapter for personal data assistant has light source that emits light beam and photo detector is electrically coupled to microprocessor

Patent Assignee: 3COM CORP (THRE-N)

Inventor: **THOMPSON C**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6065880	A	20000523	US 9836851	A	19980309	200047	B

Priority Applications (No Type Date): US 9836851 A 19980309

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6065880	A		10	G06F-013/00	

Abstract (Basic): US 6065880 A

NOVELTY - A microprocessor (38) is electrically coupled to an interface connector (36) that can be removably electrically coupled with the PDA (12). A light source (44) is configured to emit a light beam. A photo detector (56) is electrically coupled to the microprocessor.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) an electrical apparatus;

(b) and a PDA.
USE - For personal data assistant.
ADVANTAGE - Allows information to be easily downloaded into host computer without having to physically electrically couple PDA to host computer. Allows quick input of data to PDA. Enables automatic input of bar code readings into PDA, thereby enabling PDA to be effectively used for monitoring and controlling inventory or other products on which bar codes can be positioned. Minimizes size of PDA since adapter is removable.
DESCRIPTION OF DRAWING(S) - The figure is the block diagrams of the components of the adapter and the components of a computer.
PDA (12)
Interface connector (36)
Microprocessor (38)
Light source (44)
Photo detector (56)
pp; 10 DwgNo 2/5
Title Terms: PERSON; DATA; ASSIST; LIGHT; SOURCE; EMIT; LIGHT; BEAM; PHOTO; DETECT; ELECTRIC; COUPLE; MICROPROCESSOR
Derwent Class: T01; W01
International Patent Class (Main): **G06F-013/00**
File Segment: EPI

5/5/37 (Item 31 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013180801 **Image available**
WPI Acc No: 2000-352674/200031
XRPX Acc No: N00-264283
Method for relating profile data collecting during execution of optimized computer program back-to-the source language description of computer program by relating each accumulated count to actual line number of a branch instruction
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: BUZBEE W B; RUSCETTA M A; **THOMPSON C L**
Number of Countries: 026 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1004961	A2	20000531	EP 99308943	A	19991110	200031	B
US 6275981	B1	20010814	US 98190994	A	19981112	200148	
EP 1004961	B1	20030730	EP 99308943	A	19991110	200356	
DE 69909945	E	20030904	DE 609945	A	19991110	200366	
			EP 99308943	A	19991110		

Priority Applications (No Type Date): US 98190994 A 19981112
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1004961	A2	E	26	G06F-009/45	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
US 6275981	B1			G06F-009/45	
EP 1004961	B1	E		G06F-009/45	
Designated States (Regional): DE FR GB					
DE 69909945	E			G06F-009/45	Based on patent EP 1004961

Abstract (Basic): EP 1004961 A2
NOVELTY - The method involves relating each accumulated count to the actual line number of a branch instruction associated with the count and the logic line number of the basic block that contains the target instruction associated with the count.
USE - In run-time performance analysis of computer software programs compiled by optimizing compilers for correlating tun time profile data collected during execution of an optimized machine code version of program with the source language program from which the machine code version of the program is generated.

ADVANTAGE - Provides improved method of collecting data.
DESCRIPTION OF DRAWING(S) - The drawing shows a control flow graph that represents the intermediate level assembly language version of the routing 'skewed'.
pp; 26 DwgNo 1/3
Title Terms: METHOD; RELATED; PROFILE; DATA; COLLECT; EXECUTE; OPTIMUM; COMPUTER; PROGRAM; BACK; SOURCE; LANGUAGE; DESCRIBE; COMPUTER; PROGRAM; RELATED; ACCUMULATE; COUNT; ACTUAL; LINE; NUMBER; BRANCH; INSTRUCTION
Derwent Class: T01
International Patent Class (Main): **G06F-009/45**
File Segment: EPI

5/5/38 (Item 32 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012471642 **Image available**
WPI Acc No: 1999-277750/199923
XRPX Acc No: N99-208175

Computer system that provides operating system control of hardware deferral of exception in operation - indicates whether hardware should defer exception based upon at least one of first and second information, and whether instruction is speculative

Patent Assignee: INST DEV EMERGING ARCHITECTURES LLC (EMER-N)
Inventor: BURGER S G; FREUDENBERGER S M; GUPTA R; HAMMOND G; HAYS J O; KLING R M; MILLS J D; MORRIS D C; ROSS J K; **THOMPSON C L** ; HAMMOND G N
Number of Countries: 083 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9919794	A1	19990422	WO 98US21454	A	19981009	199923	B
US 5915117	A	19990622	US 97949295	A	19971013	199931	
AU 9897990	A	19990503	AU 9897990	A	19981009	199937	
EP 951672	A1	19991027	EP 98952242	A	19981009	199950	
			WO 98US21454	A	19981009		
EP 951672	B1	20030219	EP 98952242	A	19981009	200314	
			WO 98US21454	A	19981009		
DE 69811474	E	20030327	DE 611474	A	19981009	200329	
			EP 98952242	A	19981009		
			WO 98US21454	A	19981009		
AU 758574	B	20030327	AU 9897990	A	19981009	200330	

Priority Applications (No Type Date): US 97949295 A 19971013
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9919794	A1	E	49	G06F-009/38	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
US 5915117	A			G06F-009/38	
AU 9897990	A			G06F-009/38	Based on patent WO 9919794
EP 951672	A1	E		G06F-009/38	Based on patent WO 9919794
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
EP 951672	B1	E		G06F-009/38	Based on patent WO 9919794
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
DE 69811474	E			G06F-009/38	Based on patent EP 951672 Based on patent WO 9919794
AU 758574	B			G06F-009/38	Previous Publ. patent AU 9897990 Based on patent WO 9919794

Abstract (Basic): WO 9919794 A
NOVELTY - A device is used for communicating second information,

between an operating system and an application, about whether the operating system will attempt to recover from the exception prior to deferral. A device is used for communicating third information, between the operating system and the hardware, that indicates whether the hardware should defer the exception based upon at least one of the first information and the second information, and whether the instruction is speculative. DETAILED DESCRIPTION - One of the bits is the instruction translation look-aside buffer (TLB) (331) entry called ITLB.ed (the ed is for exception deferral). This bit controls whether any exceptions on any speculative loads contained in the present page can be deferred in hardware. By defining a bit (321) in the TLB entry to control hardware exception deferral, different software modules (which map to different pages in memory) can set this bit independently thus allowing each module to independently include recovery code. The inventive mechanism also uses multiple bits in a control register (DCR) (332). The preferred embodiment is to have one bit per exception type. Other mappings of bits to exception types are possible, e.g. a single bit controlling multiple exception types. Given the one-to-one correspondence between OCR bits and exception types, the operating system (OS) (320) has the flexibility to select (322) which exception types can be deferred in hardware and which ca nnot.

USE - The invention applies to any type of speculative instruction used in operating system control of a hardware deferral of an exception that has occurred in execution of an instruction in application.

ADVANTAGE - The invention enables a mechanism to defer exceptions on speculative instructions that applies to as many forms of speculation as possible. The mechanism must posses very low latency otherwise the performance of a program compiled with speculation may actually be lower than the same program compiled without speculation. The mechanism must also place minimal restrictions on the form and the construction of software in order to allow the execution of legacy software, to minimize the impact on software developers, and to maximize the range of software implementation choices. The mechanism allows the computer system to dynamically adapt to program behaviour in order to maximize performance over the broadest possible range of software DESCRIPTION OF DRAWING(S) - The drawing a schematic diagram with system implementing operation scheme according to the present invention. (320) operating system (OS) ; (331) instruction translation look-aside buffer (TLB) ; (332) control register (DCR) .

Dwg.3/3

Title Terms: COMPUTER; SYSTEM; OPERATE; SYSTEM; CONTROL; HARDWARE; OPERATE; INDICATE; HARDWARE; DEFER; BASED; ONE; FIRST; SECOND; INFORMATION; INSTRUCTION

Derwent Class: T01

International Patent Class (Main): **G06F-009/38**

File Segment: EPI

5/5/39 (Item 33 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012471015 **Image available**

WPI Acc No: 1999-277123/199923

Related WPI Acc No: 2000-654935; 2001-662400

XRPX Acc No: N99-207752

Method storing register contents in memory resource by storing N bits of contents at 1st location in resource and M bits to collection storage facility, sees if facility has preset number of bits

Patent Assignee: IDEA CORP (IDEA-N); INST DEV EMERGING ARCHITECTURES LLC (EMER-N)

Inventor: COUTANT C A; ROSS J K; **THOMPSON C L** ; ZAHIR A R

Number of Countries: 084 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9917207	A1	19990408	WO 98US20746	A	19980930	199923	B
AU 9895991	A	19990423	AU 9895991	A	19980930	199935	

EP 1019829	A1	20000719	EP 98949726	A	19980930	200036
			WO 98US20746	A	19980930	
CN 1278344	A	20001227	CN 98810765	A	19980930	200123
US 6263401	B1	20010717	US 97940834	A	19970930	200142

Priority Applications (No Type Date): US 97940834 A 19970930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9917207	A1	E	24	G06F-012/02	

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9895991	A			Based on patent WO 9917207
EP 1019829	A1	E	G06F-012/02	Based on patent WO 9917207

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

CN 1278344	A		G06F-012/02
US 6263401	B1		G06F-009/315

Abstract (Basic): WO 9917207 A1

NOVELTY - The apparatus transfers data from a register stack (86) to memory and has a temporary storage facility (108 or 110). Transfer logic transfers N bits of 1st register contents in the stack to a memory 1st location, and M bits to 1st location in the temporary facility. When preset number of data transfers have occurred logic transfers temporary facility accumulated contents to 2nd location in memory.

USE - For providing a method and apparatus for transferring data between a register stack and a backing store defined in the memory of the microprocessor.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic representation of apparatus for transferring data between a register stack and a memory resource.

register stack (86)
temporary storage facilities (108 and 110)
pp; 24 DwgNo 3/6

Title Terms: METHOD; STORAGE; REGISTER; CONTENT; MEMORY; RESOURCE; STORAGE; N; BIT; CONTENT; LOCATE; RESOURCE; BIT; COLLECT; STORAGE; FACILITY; FACILITY; PRESET; NUMBER; BIT
Derwent Class: T01
International Patent Class (Main): **G06F-009/315 ; G06F-012/02**
File Segment: EPI

```
Set     Items   Description
S1      10188   AU=(LITTFIN, J? OR LITTFIN J? OR THOMPSON, C? OR THOMPSON -
             C?)
S2          0   S1 AND INVARI?()PROPERTY
S3         10   S1 AND COMPUTER()PROGRAM
S4          2   S1 AND DATA()STRUCTURE
S5          2   S1 AND PIPELINING
S6          0   S1 AND LOOP?()INVARIANT?
S7         14   S3 OR S4 OR S5
File   2:INSPEC 1969-2004/May W2
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/May W3
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/May W2
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/May W2
         (c) 2004 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/Apr
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/May W3
         (c) 2004 BLDSC all rts. reserv.
File  92:IHS Intl.Stds.& Specs. 1999/Nov
         (c) 1999 Information Handling Services
File  94:JICST-EPlus 1985-2004/Apr W3
         (c)2004 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/May W1
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Apr
         (c) 2004 The HW Wilson Co.
File 103:Energy SciTec 1974-2004/May B1
         (c) 2004 Contains copyrighted material
File 144:Pascal 1973-2004/May W2
         (c) 2004 INIST/CNRS
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 239:Mathsci 1940-2004/Jun
         (c) 2004 American Mathematical Society
File 275:Gale Group Computer DB(TM) 1983-2004/May 17
         (c) 2004 The Gale Group
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 647:CMP  Computer Fulltext 1988-2004/May W2
         (c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2004/May W2
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/May 16
         (c) 2004 The Dialog Corp.
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Set     Items   Description
S1     281565   LOOP? OR (ITERATIVE OR GROUP)()STATEMENT? OR PIPELIN? OR L-
            OOP()INVARIANT
S2     108852   RUNTIME OR RUN()TIME OR EXECUTION
S3    4528952   PERFORM? OR WORK? OR FUNCTION? OR OPERATE?
S4    2097439   CHECK? OR VERIFY? OR TEST? OR MEASURE? OR INSPECT? OR ANAL-
            YS? OR ANALYZ? OR EXAMIN? EVALUAT? OR INTERROGAT?
S5    1724975   RANGE OR AREA OR REALM OR SCOPE OR SPHERE
S6       3534   S1 AND S2
S7       1526   S1 AND S3 AND S4 AND S5
S8         42   S6 AND S7
S9         36   S8 AND IC=G06F?
S10        20   S9 AND IC=G06F-009?
S11         6   S8 AND MC=(T01-F05A OR T01-J20C OR T01-S03)
S12        23   S10 OR S11
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200431
         (c) 2004  Thomson Derwent
```

12/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06496335 **Image available**
METHOD AND DEVICE FOR EXECUTING VERSIONING FOR **LOOP** , METHOD & DEVICE FOR COLLECTING INFORMATION ABOUT ARRANGED **RANGE CHECK** IN BASIC BLOCK, METHOD FOR MODIFYING, OPTIMIZING ARRANGED **RANGE CHECK** , GENERATING ARRANGED **RANGE CHECK** CODE, METHOD AND DEVICE FOR ELIMINATING UNNECESSARY ARRANGED **RANGE CHECK** , METHODS FOR SELECTING, MODIFYING, COLLECTING, DISPOSE-JUDGING ARRANGED **RANGE CHECK**

PUB. NO.: 2000-081983 [JP 2000081983 A]
PUBLISHED: March 21, 2000 (20000321)
INVENTOR(s): KAWAHITO MOTOHIRO
YASUE TOSHIAKI
KOMATSU HIDEAKI
APPLICANT(s): INTERNATL BUSINESS MACH CORP (IBM)
APPL. NO.: 10-370460 [JP 98370460]
FILED: December 25, 1998 (19981225)
PRIORITY: 10-195316 [JP 98195316], JP (Japan), July 10, 1998 (19980710)
INTL CLASS: **G06F-009/45**

ABSTRACT
PROBLEM TO BE SOLVED: To remove unnecessary arranged **range check** by collecting arranged **range check** information by using data flow **analysis** , etc., and **performing** move up of the **check** , etc.

SOLUTION: C-GEN[B] is collected according to a specified condition in the reverse order of **execution** in respective basic blocks B (110) and information about the C- GEN[B] is stored in a storage device. And the C-GEN[B] is propagated as adding necessary correction in the order of post order traversal for priority search of depth, C-IN [B] of the respective basic blocks B (C120) is generated and information about the C-IN[B] is stored in the storage device. Finally, a **check** code for versioning and an **execution** code in respective **execution** states are generated in front of a **loop** by using the C-IN[B] (130). The **check** code and the **execution** code are stored in the storage device for **execution** . Thus, the arranged **range check** in the **loop** is removed.

12/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06282651 **Image available**
CALCULATION DIVISION OPTIMIZING METHOD FOR PARALLEL COMPUTER

PUB. NO.: 11-224240 [JP 11224240 A]
PUBLISHED: August 17, 1999 (19990817)
INVENTOR(s): URAKAWA JUNICHI
KOBAYASHI ATSUSHI
KUROSAWA TAKASHI
NEGISHI KIYOSHI
APPLICANT(s): HITACHI LTD
HITACHI TOHOKU SOFTWARE KK
APPL. NO.: 10-025350 [JP 9825350]
FILED: February 06, 1998 (19980206)
INTL CLASS: **G06F-015/16** ; **G06F-009/45**

ABSTRACT
PROBLEM TO BE SOLVED: To generate a conversion program to optimize calculation by discriminating the repetition **range** of a **loop** when an arithmetic operation to use an array element that an adjacent process has exists in the **loop** and to generate a conversion program to make a

communication between an **execution** statement in the **loop** and the array element of the adjacent process at the same time.

SOLUTION: A parallel compiler 101 consists of a syntax **analysis** part 102, a data division **analysis** part 103, a calculation division part 104, a communication generation part 106, a conversion program generation part 107, a calculation division optimization part 105 which optimizes the **loop** by dividing it into a part to use the adjacent array element and a part to use only data in its process, and **performs** code conversion for **performing** the transfer of data and the **execution** of a **loop** main body in parallel.

12/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05945355 **Image available**
OPTIMUM PARALLEL PROGRAM GENERATING METHOD

PUB. NO.: 10-228455 [JP 10228455 A]
PUBLISHED: August 25, 1998 (19980825)
INVENTOR(s): HIROOKA TAKASHI
OTA HIROSHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-031668 [JP 9731668]
FILED: February 17, 1997 (19970217)
INTL CLASS: [6] **G06F-015/16** ; **G06F-009/45**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)

ABSTRACT

PROBLEM TO BE SOLVED: To accelerate the processing speed of a parallel program by generating an optimum parallel program into which a code that decides date division information at the time of executing is inserted.

SOLUTION: A data dividing part 6 contains a dynamic data division deciding part 7 which detects a dynamic variable that is related to the decision of data division from an intermediate word 91 and data division information 92, **performs** a dynamic data division **analysis** and outputs dynamic data division deciding information 96. It further contains a dynamic data division deciding code generating part 8 which inputs the information 96 and generates a dynamic data division deciding code. It detects a declaration **measure** of each data in a sequential executing source program 1 that is inputted in the part 6, the action **range** of a **loop** control variable and the dynamic information among reference patterns. A parallel program into which an **execution** time deciding code is inserted is generated by recording a part that dynamically decides in the information 92 and generating the **execution** time deciding code to the part that dynamically decides in the information 92.

12/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

05499899 **Image available**
PROGRAM TUNING SYSTEM BY **RANGE** INDICATION

PUB. NO.: 09-114699 [JP 9114699 A]
PUBLISHED: May 02, 1997 (19970502)
INVENTOR(s): TSURUGASAKI TOSHIHIRO
AIDA KAZUHIRO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP

(Japan)
APPL. NO.: 07-266805 [JP 95266805]
FILED: October 16, 1995 (19951016)
INTL CLASS: [6] **G06F-011/28** ; **G06F-009/06** ; **G06F-011/34**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)

ABSTRACT

PROBLEM TO BE SOLVED: To gather and display the dynamic tuning information of only a pertinent tuning **range** and to support the tuning operation of a program by indicating a **range** to **perform** the tuning operation of a source program.

SOLUTION: For a source program 101, a tuning **range** indication part 102 generates a tuning **range** specified source program 103 and a compiler 104 generates tuning **range** information 105. A tuning control part 110 and a tuning information gathering part 111 execute a **measurement** program 106 while referring to the tuning **range** information 105 and gather the tuning information 112. After **execution** is ended, a tuning display part 113 **performs** editing by a tuning **range** unit and a **loop** unit and **performs** visible display on a display screen 108.

12/5/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

05239125 **Image available**
PROGRAM DIVIDING METHOD

PUB. NO.: 08-194625 [JP 8194625 A]
PUBLISHED: July 30, 1996 (19960730)
INVENTOR(s): UMEHARA KIYOMI
SATO MAKOTO
YAMAMOTO FUJIO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-019674 [JP 9519674]
FILED: January 12, 1995 (19950112)
INTL CLASS: [6] **G06F-009/45** ; **G06F-015/16**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)

ABSTRACT

PURPOSE: To convert a successive program for single processor to a divided program for multiprocessor not to execute any useless **loop** repetition.

CONSTITUTION: A successive source program 101 with data dividing instruction is inputted, translated to an intermediate word 103, registered on a dictionary 104 and set to data division information 105. In program dividing processing 106, these elements 103-105 are inputted and deciding processing 107 of out-of- **loop** sentence **execution** PE and **loop range** dividing processing 108 are executed. In the processing 108, executing **loop range** deciding processing 109 for respective sentences inside the **loop** and **loop range** deciding processing 110 are executed. The result of the processing 106 is stored as program division information 111 and added to the intermediate word 103. Next, the elements 103-105 and 111 are inputted, non-local data are **analyzed** , non-local data **analysis** information 112 is set, inter-processor communication generating processing 113 is **performed** and the result is added to the intermediate word 103. Finally, the elements 103-105 and 111 are inputted, node program generating processing 114 is **performed** and a node program 115 for each PE is outputted.

12/5/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

04821874 **Image available**
ARRAY ELEMENT ACCESS SYSTEM AND INFORMATION PROCESSOR

PUB. NO.: 07-114474 [JP 7114474 A]
PUBLISHED: May 02, 1995 (19950502)
INVENTOR(s): TOYAMA KEISUKE
HASHIMOTO AKIRA
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI MICOM SYST KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-260640 [JP 93260640]
FILED: October 19, 1993 (19931019)
INTL CLASS: [6] **G06F-009/45**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)

ABSTRACT

PURPOSE: To increase opportunity to reduce the number of **execution** instructions of a **loop** by **performing** the addtion of an index and completion discrimination by the same instruction by extending the applicable **range** of an update branch instruction in an optimizing system for the compiler of a computer program.

CONSTITUTION: In a step 101, the facts that the update operation of a control variable in the **loop** is repeatedly **performed** once every update **execution** , that the index is updated by the same quantity every repetition, that the value of the control variable at a time when it goes out of the **loop** is not used anywhere, and that the reference to the control variable is limited to only access to an array element are **checked** . In a step 102, the address of the final element is calculated, and the maximum value of an index equation can be found. In a step 103, -N that is the result of subtraction of the number N of times of repetition from an initial value 0 is set as the initial value of the control variable, and in a step 104, the access instruction of the array element is generated. In a step 105, the update branch instruction is generated, and a code to **perform** the completion discrimination of the **loop** is generated.

12/5/7 (Item 7 from file: 347)

04274070 **Image available**
COMPUTER LANGUAGE PROCESSING METHOD

PUB. NO.: 05-265770 [JP 5265770 A]
PUBLISHED: October 15, 1993 (19931015)
INVENTOR(s): NAKAHIRA NAOJI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-061984 [JP 9261984]
FILED: March 18, 1992 (19920318)
INTL CLASS: [5] **G06F-009/45**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1679, Vol. 18, No. 39, Pg. 96, January 20, 1994 (19940120)

ABSTRACT

PURPOSE: To improve the **execution performance** of a program by **performing** optimization, by which data in a multiplex **loop** can be accessed at a high speed, in a wide **range** .

CONSTITUTION: With respect to the computer language processing method which **performs** the optmization processing at the time of translation to an object program 15 of a program 10 which is **operated** on a computer having a hierarchical memory, **loops** having a tight structure are detected in an

optimization processing part 13 to recognize **loops** which can be blocked. Data overlap **analysis** is used to substitute **loops** so that the access distance of array data in the innermost **loop** is shortened. Candidate arrays which can be blocked are extracted, and a division object array and a division object index are determined from candidate arrays. The divided block length is so determined that arrays after division can be stored in a cache memory, and the **loop** is transformed.

12/5/8 (Item 8 from file: 347)

03589057 **Image available**
VECTORIZATION PROCESSING SYSTEM

PUB. NO.: 03-251957 [JP 3251957 A]
PUBLISHED: November 11, 1991 (19911111)
INVENTOR(s): FUJIMAKI MIDORI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-049884 [JP 9049884]
FILED: February 28, 1990 (19900228)
INTL CLASS: [5] **G06F-015/347 ; G06F-009/45**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1308, Vol. 16, No. 50, Pg. 149, February 07, 1992 (19920207)

ABSTRACT

PURPOSE: To permit vectorization of a sentence group and to shorten the program executing time by deforming an intermediate text to a scalar variable having the reliance between the data conflicting with each other.
CONSTITUTION: A sentence structure **analyzing** means 21 of a compiler 2 reads a source program 1 and produces an intermediate text 26. A data reliance deciding means 22 of a vectorization means 4 detects all array elements and scalar variables out of the text 26 in regard of the pool structure contained in the program 1. Then the means 22 turns off the data reliance flag contained in the element data and turns on the data reliance flag of an element table corresponding to the element having the data reliance conflicting with the parallel **execution** among those elements included in a **loop** . A sentence replacement processing means 23 **performs** the replacement of the sentences including the corresponding elements to a sentence group having the conflicting data reliance. A variable data reliance dissolving means 24 deforms the text 26 and handles the conflict scalar variable in the same way as the one-dimensional array element using a vector **work area** . Thus the conflict is dissolved. A code generating means 25 generates an object program 3 from the text 26.

12/5/9 (Item 9 from file: 347)

03428136 **Image available**
PARALLEL COMPILE METHOD

PUB. NO.: 03-091036 [JP 3091036 A]
PUBLISHED: April 16, 1991 (19910416)
INVENTOR(s): TANAKA GIICHI
KOBAYASHI ATSUSHI
IWAZAWA KYOKO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-227346 [JP 89227346]
FILED: September 04, 1989 (19890904)
INTL CLASS: [5] **G06F-009/45**

JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1225, Vol. 15, No. 270, Pg. 83, July 09, 1991 (19910709)

ABSTRACT

PURPOSE: To enlarge the objective **range** of parallelizing by classifying simple variables and arrangement in a multiple **loop** from the viewpoint of parallelizing in a parallelizing processing and introducing **work** variables and **work** arrangement to a case that parallelizing can not be executed conventionally.

CONSTITUTION: A FORTRAN program 51 is converted to an intermediate word 53 by a syntax **analysis** processing 52. In an intermediate processing 54, this word is inputted and data dependency **analysis** is executed. Then, a data dependency graph 57 is prepared and control dependency **analysis** is executed. Afterwards, a control dependency graph 58 is prepared and in the parallelizing processing, sections to be parallelly executed by plural processors are found out. Then, an optimumizing processing is executed and the converted intermediate word 53 is outputted. Next, in a code generation processing 55, a main memory is allocated to the variable and an object code 56 is generated. Thus, concerning the intermediate processing 54, the wider **range** is parallelized, the **execution** ability of the object code 56 is improved and the objective **range** of parallelizing is enlarged.

12/5/10 (Item 10 from file: 347)

03126077 **Image available**
VECTORIZING PROCESSING SYSTEM

PUB. NO.: 02-101577 [JP 2101577 A]
PUBLISHED: April 13, 1990 (19900413)
INVENTOR(s): FUJIMAKI MIDORI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-255597 [JP 88255597]
FILED: October 11, 1988 (19881011)
INTL CLASS: [5] **G06F-015/347** ; **G06F-009/45**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1072, Vol. 14, No. 313, Pg. 145, July 05, 1990 (19900705)

ABSTRACT

PURPOSE: To enable vectorizing even in a case where reference exists to the scalar variable of the left side of an assignment statement by allotting a vectoring **work area** to the regressive operation of a recurrence formula can be applied.

CONSTITUTION: When a **loop** structure is **analyzed** in the course of compling, and data dependence incompatible with parallel **execution** exists, a regressive operation processing part 223 is started. The regressive operation pattern recognizing part 2231 of the processing part 223 investigates the structure of a formula, and detects the statement of the regressive operation with the specified pattern of an inner product/total sum for the scalar variable. A definition/ reference position relation investigating part 2232 investigates definition/reference position relation in a **loop** for the scalar variable of the detected statement. As the result of the investigation, when the reference exists for the scalar variable of the left side of the assignment statement after the statement of the regressive operation, a regressive operation vectorizing processing part 2233 allots the vectorizing **work area** to this scalar variable, and transforms it into the statement where the regressive operation of the recurrence formula can be applied.

12/5/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

01886762 **Image available**
SEQUENCING SYSTEM OF INSTRUCTION

PUB. NO.: 61-100862 [JP 61100862 A]
PUBLISHED: May 19, 1986 (19860519)
INVENTOR(s): AOKI MASAKI
NAKADA HIROSHI
HIRABAYASHI TOSHIHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-213315 [JP 84213315]
FILED: October 12, 1984 (19841012)
INTL CLASS: [4] **G06F-015/347 ; G06F-009/38 ; G06F-009/44**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 500, Vol. 10, No. 282, Pg. 59, September 25, 1986 (19860925)

ABSTRACT

PURPOSE: To enhance the parallelism between DO **loops** made into vectors and other **range** and to increase the efficiency of **execution** by grasping its data dependency in wide **range** and making the optimum sequencing process.

CONSTITUTION: Data **analyzed** in a source **analyzing** section 1 is given to an address allocating section 2, and there, memory **area** is allotted, and initial values are given to arrays and variables. A vector making section 3 converts DO **loops** to vector instruction strings, and a sequencing processing section 4 grasps its data dependency in wide **range** , and makes the optimum sequencing of instruction to the data dependency by using a pipe line ID or synchronizing instruction. An intermediate text optimizing section 5 makes optimizing after making into vectors, and a register allotting section 6 **performs** processing such as allotting data to registers. An instruction generating section 7 converts an intermediate **test** to a machine language instruction.

12/5/12 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014037828
WPI Acc No: 2001-522041/200157
XRPX Acc No: N01-386908
Computer method for providing early warning has early warning code inserted in its program code at locations determined by a control flow representation to monitor for specified events
Patent Assignee: INCERT SOFTWARE CORP (INCE-N)
Inventor: AGARWAL A; AYERS A E; SCHOOLER R
Number of Countries: 093 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200148608	A2	20010705	WO 2000US34825	A	20001220	200157	B
AU 200124473	A	20010709	AU 200124473	A	20001220	200164	

Priority Applications (No Type Date): US 99474679 A 19991229
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200148608	A2	E	32	G06F-011/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT

RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
AU 200124473 A G06F-011/00 Based on patent WO 200148608

Abstract (Basic): WO 200148608 A2

NOVELTY - Locations in a program are selected using changes and **test** coverage and control flow and data **analysis** and early warning codes monitoring for an event are inserted in the selected locations. On detecting the event, the early warning code provides an early warning or issues an early action. In one embodiment an early warning is issued if the value of an argument to a selected **function** is outside a predetermined **range** . Early warnings may be issued if a **loop** is executed more than a predetermined number of times or when the time elapsed between the **execution** of two points in the program exceeds a given value or if the program enters a block of untested code. The warning may be issued by sending an e-mail to an operator.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for
(a) a computer system for issuing an early warning
(b) a computer program product for issuing an early warning
(c) and a computer memory configured to provide an early warning.

USE - In data processing systems.

ADVANTAGE - Provides an early warning in advance of any failure or crash.

pp; 32 DwgNo 0/6

Title Terms: COMPUTER; METHOD; EARLY; WARNING; EARLY; WARNING; CODE; INSERT ; PROGRAM; CODE; LOCATE; DETERMINE; CONTROL; FLOW; REPRESENT; MONITOR; SPECIFIED; EVENT
Derwent Class: T01
International Patent Class (Main): G06F-011/00
File Segment: EPI

12/5/13 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013337323 **Image available**
WPI Acc No: 2000-509262/200046
XRPX Acc No: N00-376880

Compiler for computer, writes-in the lead address value of condition process, referring to which execution **of** loop **process in a program is** performed

Patent Assignee: TOSHIBA AVE KK (TOSA); TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000194569	A	20000714	JP 98371613	A	19981225	200046	B

Priority Applications (No Type Date): JP 98371613 A 19981225
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000194569	A		16	G06F-009/45	

Abstract (Basic): JP 2000194569 A

NOVELTY - The source program consists of condition branch instruction **loop** , provided between a common process and condition process. The lead address value of the condition process is written by lead address setting unit (126), referring to which **execution** of the **loop** is **performed** by jump instruction converter (127).

DETAILED DESCRIPTION - The **loop** process portion is extracted from program by optimization unit (123). The recording **area** of the variable that controls **loop** frequency is **analyzed** by recording **area analysis** unit (125) for selecting the **area** to record the lead address value of condition process. INDEPENDENT CLAIMS are also included for the following:

(a) compile procedure;

(b) compile program;
(c) target program
USE - In e.g. compiler for computer.
ADVANTAGE - **Execution** of a **loop** in a program is reduced, thus the process time of the system is reduced, thereby reducing the capacity of target program.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of compiler.
Optimization unit (123)
Recording **area analysis** unit (125)
Lead address setting unit (126)
Jump instruction converter (127)
pp; 16 DwgNo 1/14
Title Terms: COMPILE; COMPUTER; WRITING; LEAD; ADDRESS; VALUE; CONDITION; PROCESS; REFER; EXECUTE; **LOOP** ; PROCESS; PROGRAM; **PERFORMANCE**
Derwent Class: T01
International Patent Class (Main): **G06F-009/45**
International Patent Class (Additional): **G06F-009/42**
File Segment: EPI

12/5/14 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012899224 **Image available**
WPI Acc No: 2000-071059/200006
Related WPI Acc No: 1999-228858
XRPX Acc No: N00-055478
Signed data signal optimization apparatus for superscalar pipelined **processor**
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: VOLKONSKY V Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5996056	A	19991130	US 97880335	A	19970623	200006 B
			US 97881511	A	19970624	

Priority Applications (No Type Date): US 97880335 A 19970623; US 97881511 A 19970624
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5996056	A		8	G06F-015/16	Div ex application US 97880335 Div ex patent US 5887181

Abstract (Basic): US 5996056 A
NOVELTY - An intermediate signal from two image signals, represented as signed 8-bit integer is obtained using registers. By bit wise shifting, it is **checked** whether the intermediate signal is within the **range** of positive and negative overflow state, and sets a mask signal to have 8 lower bits in OFF position or ON position, accordingly.
DETAILED DESCRIPTION - The processor includes registers in graphics unit (38) for storing two image signals and obtaining intermediate signal. By bit wise shifting of intermediate signal to four positions to right a masking signal with a value 8, is obtained. By dividing the intermediate signal by 16 and storing the dividend, the processor determines the positive or negative overflow state. The integer **execution** unit (28) has arithmetic and logic units for **performing** arithmetic, logical and shift operations. Bit wise AND operation is **performed** on intermediate signal with mask signal to obtain translated data signal which is ORed bit wise with another mask signal.
INDEPENDENT CLAIMS are also included for the following:
(a) signed data signal optimization method;
(b) signed data signal optimization program on a computer readable medium.
USE - For **checking** audio and pixel data of multimedia signal in

computer system using superscalar **pipelined** processor.

ADVANTAGE - Since the resulting pixel or signed 8-bit integers remain within the boundaries of signed 8-bit integers, the use of conditional branches is eliminated, as three shift operations, two logic multiplication's and an addition operation is employed. Thereby, instruction throughput of processor is improved and efficiency of instruction **pipelining** is enhanced.

DESCRIPTION OF DRAWING(S) - The figure shows schematic block diagram of superscalar **pipelined** processor.

Integer **execution** unit (38)

Graphics unit (38)

pp; 8 DwgNo 2/3

Title Terms: SIGN; DATA; SIGNAL; APPARATUS; PIPE; PROCESSOR

Derwent Class: T01

International Patent Class (Main): G06F-015/16

File Segment: EPI

12/5/15 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012099708 **Image available**

WPI Acc No: 1998-516619/199844

XRPX Acc No: N98-403955

Optimum parallel execution program generation method using parallel conversion compiler for distributed parallel processors - involves outputting dynamic data division judging information based on dynamic information utilised for data division, according to dynamic data tally rule to generate code

Patent Assignee: HITACHI LTD (HITA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10228455	A	19980825	JP 9731668	A	19970217	199844	B

Priority Applications (No Type Date): JP 9731668 A 19970217

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10228455	A		13	G06F-015/16	

Abstract (Basic): JP 10228455 A

The method involves inputting a source program (1) sequentially and **performing** syntactic **analysis** . A data division **analysis** is **performed** using the syntactic **analysis** information. A program division information is generated by **performing** division of the **loop** repetition **range** from the syntactic **analysis** information and data division information. A communication information is produced from syntactic **analysis** information, data division information and program division information. The parallel **execution** program is output based on the syntactic **analysis** information, data, program division information and communication information.

During data division process the information sequentially utilised for data division is extracted from the source program. A dynamic information is detected from the information utilised for data division. A dynamic data division judging information is output based on the detected dynamic information, according to a dynamic data tally rule to generate a code.

ADVANTAGE - Improves processing speed.

Dwg.1/16

Title Terms: OPTIMUM; PARALLEL; EXECUTE; PROGRAM; GENERATE; METHOD; PARALLEL; CONVERT; COMPILE; DISTRIBUTE; PARALLEL; PROCESSOR; OUTPUT; DYNAMIC; DATA; DIVIDE; JUDGEMENT; INFORMATION; BASED; DYNAMIC; INFORMATION; UTILISE; DATA; DIVIDE; ACCORD; DYNAMIC; DATA; TALLY; RULE; GENERATE; CODE

Derwent Class: T01

International Patent Class (Main): **G06F-015/16**

International Patent Class (Additional): **G06F-009/45**
File Segment: EPI

12/5/16 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011382823 **Image available**
WPI Acc No: 1997-360730/199733
XRPX Acc No: N97-299787
Computer program execution **cost** analysis **- by computing** execution **cost of computer program** analysed **using** performance analysis **program, according to loop processing frequency and array operation**
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9152982	A	19970610	JP 95311814	A	19951130	199733	B

Priority Applications (No Type Date): JP 95311814 A 19951130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9152982	A		13		

Abstract (Basic): JP 9152982 A

The method involves using a **performance analysis** program to **analyse** a computer program at a sentence number table (13). The sentence number table stores the relative address and the head address of a source program sentence number. An **execution** formal program which translates the source program is obtained. A **loop** information table (14) stores the sentence number of a **loop** processing program to **perform** array operation correction. The **execution** of the **execution** formal program is interrupted to search for a program sentence under **execution** .

The relative address and the head address of the **area** maintaining the program is obtained. Based on the relative address, the sentence number of the program sentence under **execution** is obtained referring to the sentence number table. The modality of the program sentence is searched referring to the **loop** information table. The **execution** cost of the computer program is computed based on the **loop** processing **execution** frequency and the array operation.

ADVANTAGE - Efficiently updates computer program.

Dwg.1/9

Title Terms: COMPUTER; PROGRAM; EXECUTE; COST; **ANALYSE** ; COMPUTATION; EXECUTE; COST; COMPUTER; PROGRAM; **ANALYSE** ; **PERFORMANCE** ; **ANALYSE** ; PROGRAM; ACCORD; **LOOP** ; PROCESS; FREQUENCY; ARRAY; **OPERATE**
Derwent Class: T01
International Patent Class (Main): G06F-011/34
File Segment: EPI

12/5/17 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011079319 **Image available**
WPI Acc No: 1997-057243/199706
Division calculation optimisation processing using electronic computer partic. for distributed parallel machines - using compiler to convert source program counter with divided data direction to source program for distribute memory store contg. parallel library
Patent Assignee: HITACHI LTD (HITA)
Inventor: SATO M; UMEHARA K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

JP 8305672 A 19961122 JP 95110473 A 19950509 199706 B
US 5781777 A 19980714 US 96642676 A 19960503 199835

Priority Applications (No Type Date): JP 95110473 A 19950509
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 8305672 A 33 G06F-015/16
US 5781777 A G06F-009/45

Abstract (Basic): JP 8305672 A

The processing method uses a parallel conversion compiler including a syntax parsing unit (102), a data division and **analysis** device (103), a calculation divider (104) and a communication device (105). The data division device converts a program counter to a parallel counter for providing certain processes. An array element is assigned on **analysing** the program counter with the data division directions.

A sentence is processed based on the relation between the rule and the array subscript which connect the array and a sentence and a **loop** control variable. The **execution range** of the sentence which is with **range** of the **loop** control variable is determined. a non-transposition section sequence processing is **performed** , and a **loop** duplicate processing is **performed** in the original **loop** .

Dwg.1/40

Title Terms: DIVIDE; CALCULATE; OPTIMUM; PROCESS; ELECTRONIC; COMPUTER; DISTRIBUTE; PARALLEL; MACHINE; COMPILE; CONVERT; SOURCE; PROGRAM; COUNTER ; DIVIDE; DATA; DIRECTION; SOURCE; PROGRAM; DISTRIBUTE; MEMORY; STORAGE; CONTAIN; PARALLEL; LIBRARY
Derwent Class: T01
International Patent Class (Main): **G06F-009/45 ; G06F-015/16**
International Patent Class (Additional): **G06F-009/45**
File Segment: EPI

12/5/18 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011055956 **Image available**
WPI Acc No: 1997-033880/199703
XRPX Acc No: N97-028640

Compiling appts. for converting source program into machine or assembly language - has function to analyse overlaps of memory addresses of two or more data expressions and generates paths when overlap of addresses is obscure

Patent Assignee: FUJITSU LTD (FUIT)
Inventor: HAYASHI M; NAKAHIRA T
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 5581762 A 19961203 US 94202580 A 19940228 199703 B

Priority Applications (No Type Date): JP 93115609 A 19930518
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 5581762 A 23 G06F-009/44

Abstract (Basic): US 5581762 A

The compiling appts. includes a unit (2) for **analysing** a structure of an intermediate language program of a source program (11) output from a front-end unit (1), and for recognising program units constituting **loops** . A unit (3) **analyses** a **scope** of declarations of respective data expressions in the **loops** . A unit (4) statically **analyses** an overlap of two memory addresses of data expressions of each pair and outputs an overlap **analysis** result.

A unit (5) inserts an instruction to compare the two memory addresses of data expressions of each pair whose overlap is judged to be obscure, for generating a number of paths defined by combinations of

conditions whether or not the two memory addresses of data expressions of each pair overlap, and for generating an instruction to branch to one of the number of paths according to a comparison result obtained by the instruction in an **execution** of a compiled program. A unit (6) respectively optimises the number of paths generated by the aliasing address comparison instruction generating unit.

ADVANTAGE - Can carry out optimisation of data expressions whose overlaps are judged to be obscure. Can output more efficient object program.

Dwg.3/14

Title Terms: COMPILE; APPARATUS; CONVERT; SOURCE; PROGRAM; MACHINE; ASSEMBLE; LANGUAGE; **FUNCTION** ; **ANALYSE** ; OVERLAP; MEMORY; ADDRESS; TWO; MORE; DATA; EXPRESS; GENERATE; PATH; OVERLAP; ADDRESS; OBSCURE

Derwent Class: T01

International Patent Class (Main): **G06F-009/44**

File Segment: EPI

12/5/19 (Item 8 from file: 350)

011002545 **Image available**

WPI Acc No: 1996-499494/199650

XRPX Acc No: N96-421307

Memory operation reordering for instruction level parallelism in VLIW processor - involves checking **decoded instructions for out of order instructions and setting exception bits depending on nature of instruction**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)

Inventor: EBICIOGLU M K; LUICK D A; MORENO J H; SILBERMAN G M; WINTERFIELD P B; EBCIOGLU M K

Number of Countries: 005 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 742512	A2	19961113	EP 96106145	A	19960419	199650	B
JP 8314721	A	19961129	JP 9698035	A	19960419	199707	
US 5625835	A	19970429	US 95435411	A	19950510	199723	
JP 3096423	B2	20001010	JP 9698035	A	19960419	200052	

Priority Applications (No Type Date): US 95435411 A 19950510

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 742512	A2	E	13	G06F-009/38	
Designated States (Regional): DE FR GB					
JP 8314721	A		12	G06F-009/38	
US 5625835	A		10	G06F-009/38	
JP 3096423	B2		13	G06F-009/38	Previous Publ. patent JP 8314721

Abstract (Basic): EP 742512 A

The memory reordering method involves decoding instructions issued by a processor. If a decoded instruction is an out of order load instruction it is determined if the instruction generates an exception. A delayed exception bit associated with a target register of the load instruction for an out of order load instruction generating an exception is set. A memory address of an out of order load instruction not generating an exception is saved and a valid bit is set for this address. It is determined if a decoded instruction is a store operation. A **range** of memory addresses referenced by a decoded store instruction are compared with all entries in the address comparator. For each match the valid bit of the corresponding entry is set to invalid.

It is determined if a decoded instruction is a commit operation. The valid bit of the address comparator entry associated with a target register of the decoded commit operation. A delayed exception is generated if the valid bit is set to invalid. The delayed exception bit of a source register of the commit operation is simultaneously **checked**

. If the bit is set a delayed exception is generated. An exception instruction is aborted and control is transferred to an exception handler.

ADVANTAGE - Allows moving of load instructions earlier in **execution** stream allowing for arbitrary distance between reading from memory and using data loaded out of order. Not restricted to moving load operations out of **loops** and can tolerate ambiguous memory references. Provides high **performance** and integrates memory disambiguation with speculative **execution** . Copes with ambiguous store/load instructions.

Dwg.1a/2

Title Terms: MEMORY; **OPERATE** ; INSTRUCTION; LEVEL; PARALLEL; PROCESSOR; **CHECK** ; DECODE; INSTRUCTION; ORDER; INSTRUCTION; SET; BIT; DEPEND; NATURE ; INSTRUCTION
Derwent Class: T01
International Patent Class (Main): **G06F-009/38**
File Segment: EPI

12/5/20 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010565765 **Image available**
WPI Acc No: 1996-062718/199607
XRPX Acc No: N96-052514

Test **coverage measuring method for data-processing system - by using** test **coverage** measurement **program which** measures **source program counter by allotting** test **sequences for correction** range

Patent Assignee: HITACHI CHO LSI ENG KK (HISC); HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7319732	A	19951208	JP 94108056	A	19940523	199607	B
JP 3394813	B2	20030407	JP 94108056	A	19940523	200324	

Priority Applications (No Type Date): JP 94108056 A 19940523
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7319732	A		6	G06F-011/28	
JP 3394813	B2		6	G06F-011/28	Previous Publ. patent JP 7319732

Abstract (Basic): JP 7319732 A

The method uses a source program counter (110) which connects and assembles a printed-circuit board (510) designed to connect one or more other circuit boards. A **test** coverage information table is created by extracting a correction difference information (210) and an **execution** sentence information from the counter.

Afterwards, the **test** coverage information implements a **test** procedure by initially setting the correction **range** to a nonperforming state followed by a **performing** state. The **execution** path provides the regular update on the table. A **test** coverage **measurement** program (400) is designed to **test** the source program counter by easily monitoring the **test** **range** and the **test** progress situation.

ADVANTAGE - Enables easy **test** **range** distinction before **test** starts and provides **loop** to monitor easily **test** progress situation by referring to table.

Dwg.1/2

Title Terms: **TEST** ; COVER; **MEASURE** ; METHOD; DATA; PROCESS; SYSTEM; **TEST** ; COVER; **MEASURE** ; PROGRAM; **MEASURE** ; SOURCE; PROGRAM; COUNTER; ALLOT; **TEST** ; SEQUENCE; CORRECT; **RANGE**
Derwent Class: T01
International Patent Class (Main): **G06F-011/28**
International Patent Class (Additional): **G06F-009/06**
File Segment: EPI

12/5/21 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008598202 **Image available**
WPI Acc No: 1991-102234/199114
XRPX Acc No: N91-078995

High level computer interface for program development - pushes editing and validation, error processing, looping , selection, ordering and auditing down into data access

Patent Assignee: AMDAHL CORP (AMDA)
Inventor: CHONG D T; KNUDSEN H; PLAZAK Z; ROBERTSON M; TAUGHER J E; YAFFE J ; TAUGHER J
Number of Countries: 017 Number of Patents: 044
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9103791	A	19910321				199114 B
AU 9064293	A	19910408				199127
EP 489861	A1	19920617	EP 90914340	A	19900904	199225
			WO 90US5007	A	19900904	
JP 5502527	W	19930428	JP 90513420	A	19900904	199322
			WO 90US5007	A	19900904	
AU 9346083	A	19931216	AU 9064293	A	19900904	199406
			AU 9346083	A	19930903	
AU 9346084	A	19931216	AU 9064293	A	19900904	199406
			AU 9346084	A	19930903	
AU 9346082	A	19931223	AU 9064293	A	19900904	199407
			AU 9346082	A	19930903	
EP 588445	A2	19940323	EP 90914340	A	19900904	199412
			EP 93203195	A	19900904	
EP 588446	A2	19940323	EP 90914340	A	19900904	199412
			EP 93203242	A	19900904	
EP 588447	A2	19940323	EP 90914340	A	19900904	199412
			EP 93203243	A	19900904	
AU 646408	B	19940224	AU 9064293	A	19900904	199413
EP 588445	A3	19940504	EP 93203195	A	19900904	199523
EP 489861	A4	19930804	EP 90914340	A		199527
EP 588446	A3	19951115	EP 93203242	A	19900904	199618
EP 588447	A3	19960417	EP 90914340	A	19900904	199626
			EP 93203243	A	19900904	
AU 671137	B	19960815	AU 9064293	A	19900904	199641
			AU 9346082	A	19930903	
AU 671138	B	19960815	AU 9064293	A	19900904	199641
			AU 9346084	A	19930903	
AU 673682	B	19961121	AU 9064293	A	19900904	199703
			AU 9346083	A	19930903	
US 5584026	A	19961210	US 89402862	A	19890901	199704
			US 89450298	A	19891213	
			US 92830548	A	19920131	
			US 92968237	A	19921029	
			US 9329699	A	19930311	
			US 95426489	A	19950420	
US 5586329	A	19961217	US 89402862	A	19890901	199705
			US 89450298	A	19891213	
			US 92830548	A	19920131	
			US 92968237	A	19921029	
			US 9329908	A	19930311	
			US 95424234	A	19950418	
US 5586330	A	19961217	US 89402862	A	19890901	199705
			US 89450298	A	19891213	
			US 92830548	A	19920131	
			US 92968237	A	19921029	
			US 9329478	A	19930311	
			US 95424241	A	19950418	
US 5594899	A	19970114	US 89402862	A	19890901	199709
			US 89450298	A	19891213	

			US 92830548	A	19920131	
			US 92968237	A	19921029	
			US 9329902	A	19930311	
			US 94347588	A	19941201	
US 5596752	A	19970121	US 89402862	A	19890901	199710
			US 89450298	A	19891213	
			US 92830548	A	19920131	
			US 92968237	A	19921029	
			US 9329700	A	19930311	
EP 489861	B1	19970709	EP 90914340	A	19900904	199732
			WO 90US5007	A	19900904	
DE 69031040	E	19970814	DE 631040	A	19900904	199738
			EP 90914340	A	19900904	
			WO 90US5007	A	19900904	
US 5682535	A	19971028	US 89402862	A	19890901	199749
			US 92830550	A	19920131	
			US 92968474	A	19921029	
			US 9397096	A	19930726	
			US 97784736	A	19970113	
EP 588445	B1	19990519	EP 90914340	A	19900904	199924
			EP 93203195	A	19900904	
EP 588447	B1	19990519	EP 90914340	A	19900904	199924
			EP 93203243	A	19900904	
DE 69033120	E	19990624	DE 633120	A	19900904	199931
			EP 93203195	A	19900904	
DE 69033121	E	19990624	DE 633121	A	19900904	199931
			EP 93203243	A	19900904	
EP 588446	B1	19990707	EP 90914340	A	19900904	199931
			EP 93203242	A	19900904	
DE 69033203	E	19990812	DE 633203	A	19900904	199938
			EP 93203242	A	19900904	
ES 2132175	T3	19990816	EP 93203195	A	19900904	199939
ES 2132176	T3	19990816	EP 93203243	A	19900904	199939
ES 2133145	T3	19990901	EP 93203242	A	19900904	199941
CA 2284245	A1	19910302	CA 2066724	A	19900904	200015
			CA 2284245	A	19900904	
CA 2284247	A1	19910302	CA 2066724	A	19900904	200015
			CA 2284247	A	19900904	
CA 2284248	A1	19910302	CA 2066724	A	19900904	200015
			CA 2284248	A	19900904	
CA 2284250	A1	19910302	CA 2066724	A	19900904	200015
			CA 2284250	A	19900904	
CA 2066724	C	20001205	CA 2066724	A	19900904	200101
			WO 90US5007	A	19900904	
CA 2284245	C	20010206	CA 2066724	A	19900904	200111
			CA 2284245	A	19900904	
CA 2284248	C	20011204	CA 2066724	A	19900904	200203
			CA 2284248	A	19900904	
CA 2284250	C	20011204	CA 2066724	A	19900904	200203
			CA 2284250	A	19900904	
JP 3478820	B2	20031215	JP 90513420	A	19900904	200405
			WO 90US5007	A	19900904	

Priority Applications (No Type Date): US 89450298 A 19891213; US 89402862 A 19890901; US 92830548 A 19920131; US 92968237 A 19921029; US 9329699 A 19930311; US 95426489 A 19950420; US 9329908 A 19930311; US 95424234 A 19950418; US 9329478 A 19930311; US 95424241 A 19950418; US 9329902 A 19930311; US 94347588 A 19941201; US 9329700 A 19930311; US 92830550 A 19920131; US 92968474 A 19921029; US 9397096 A 19930726; US 97784736 A 19970113

Cited Patents: 1.Jnl.Ref; EP 163577; US 4791561; EP 331060; US 4860204; DE 3503119; EP 243110; GB 2126761; US 4099230

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9103791	A				

Designated States (National): AU CA JP US

Designated States (Regional): AT BE CH DE DK ES FR GB IT LU NL SE

EP 489861	A1 E	2	G06F-015/40	Based on patent WO 9103791
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI LU NL SE				
JP 5502527	W		G06F-009/06	Based on patent WO 9103791
AU 9346083	A		G06F-009/44	Div ex application AU 9064293
AU 9346084	A		G06F-015/40	Div ex application AU 9064293
AU 9346082	A		G06F-009/45	Div ex application AU 9064293
EP 588445	A2 E	84	G06F-015/413	Related to application EP 90914340
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI LU NL SE				
EP 588446	A2 E	84	G06F-009/44	Related to application EP 90914340
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI LU NL SE				
EP 588447	A2 E	87	G06F-009/44	Related to application EP 90914340
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI LU NL SE				
AU 646408	B		G06F-015/40	Previous Publ. patent AU 9064293 Based on patent WO 9103791
EP 588446	A3			Related to patent EP 489861
EP 588447	A3			Div ex application EP 90914340
AU 671137	B		G06F-009/45	Div ex application AU 9064293 Previous Publ. patent AU 9346082
AU 671138	B		G06F-015/40	Div ex application AU 9064293 Previous Publ. patent AU 9346084
AU 673682	B		G06F-009/44	Div ex application AU 9064293 Previous Publ. patent AU 9346083
US 5584026	A	72	G06F-017/30	CIP of application US 89402862 Cont of application US 89450298 Cont of application US 92830548 Div ex application US 92968237 Cont of application US 9329699
US 5586329	A	268	G06F-009/45	CIP of application US 89402862 Cont of application US 89450298 Cont of application US 92830548 Div ex application US 92968237 Cont of application US 9329908
US 5586330	A	74	G06F-009/45	CIP of application US 89402862 Cont of application US 89450298 Cont of application US 92830548 Div ex application US 92968237 Cont of application US 9329478
US 5594899	A	72	G06F-017/30	CIP of application US 89402862 Cont of application US 89450298 Cont of application US 92830548 Div ex application US 92968237 Cont of application US 9329902
US 5596752	A	73	G06F-015/00	CIP of application US 89402862 Cont of application US 89450298 Cont of application US 92830548 Div ex application US 92968237
EP 489861	B1 E	89	G06F-009/44	Based on patent WO 9103791
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI LU NL SE				
DE 69031040	E		G06F-009/44	Based on patent EP 489861 Based on patent WO 9103791
US 5682535	A	75	G06F-009/44	Cont of application US 89402862 Cont of application US 92830550 Cont of application US 92968474 Cont of application US 9397096
EP 588445	B1 E		G06F-009/44	Div ex application EP 90914340 Div ex patent EP 489861
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI LU NL SE				
EP 588447	B1 E		G06F-009/44	Div ex application EP 90914340 Div ex patent EP 489861
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI LU NL SE				
DE 69033120	E		G06F-009/44	Based on patent EP 588445
DE 69033121	E		G06F-009/44	Based on patent EP 588447
EP 588446	B1 E		G06F-009/44	Div ex application EP 90914340 Div ex patent EP 489861
Designated States (Regional): AT BE CH DE DK ES FR GB IT LI LU NL SE				
DE 69033203	E		G06F-009/44	Based on patent EP 588446
ES 2132175	T3		G06F-009/44	Based on patent EP 588445

ES 2132176	T3			G06F-009/44	Based on patent EP 588447
ES 2133145	T3			G06F-009/44	Based on patent EP 588446
CA 2284245	A1	E		G06F-017/30	Div ex application CA 2066724
CA 2284247	A1	E		G06F-009/45	Div ex application CA 2066724
CA 2284248	A1	E		G06F-009/45	Div ex application CA 2066724
CA 2284250	A1	E		G06F-009/45	Div ex application CA 2066724
CA 2066724	C	E		G06F-015/40	Based on patent WO 9103791
CA 2284245	C	E		G06F-017/30	Div ex application CA 2066724
CA 2284248	C	E		G06F-009/45	Div ex application CA 2066724
CA 2284250	C	E		G06F-009/45	Div ex application CA 2066724
JP 3478820	B2		82	G06F-009/54	Previous Publ. patent JP 5502527
					Based on patent WO 9103791

Abstract (Basic): WO 9103791 A

Objects including rules and data are stored in buffers identified by a buffer address. A current rule including a static data **area** and a modifiable data **area** is executed. The static data **area** stores object identifiers with offsets to positions in hte modifiable data **area** at which buffer addresses of buffers storing identified objects are to be located at **execution** time.

Objects are found in the buffers in response to the executing device, and buffer addresses are supplied to the modifiable data **area** at **execution** time.

ADVANTAGE - Frees programmer of explicit recognition in program of environmental parameters. (2pp Dwg.No.1/21

Title Terms: HIGH; LEVEL; COMPUTER; INTERFACE; PROGRAM; DEVELOP; PUSH; EDIT ; VALID; ERROR; PROCESS; **LOOP** ; SELECT; ORDER; AUDIT; DOWN; DATA; ACCESS

Derwent Class: T01

International Patent Class (Main): **G06F-009/06 ; G06F-009/44 ; G06F-009/45 ; G06F-009/54 ; G06F-015/00 ; G06F-015/40 ; G06F-015/413 ; G06F-017/30**

International Patent Class (Additional): **G06F-009/40 ; G06F-015/20**

File Segment: EPI

12/5/22 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007942724 **Image available**

WPI Acc No: 1989-207836/198929

XRPX Acc No: N89-158485

Buffer memory control for data processing system - using address pipeline to control addressing of buffer memory locations in response to received loading addresses

Patent Assignee: MULLER O (MULL-I); MUELLER O (MUEL-I)

Inventor: MUELLER O; MULLER O

Number of Countries: 012 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3802025	C	19890720	DE 3802025	A	19880125	198929	B
EP 325677	A	19890802	EP 88102542	A	19880222	198931	
US 4953121	A	19900828	US 88177309	A	19880405	199037	
EP 325677	B1	19930519	EP 88102542	A	19880222	199320	
EP 325677	A3	19920715	EP 88102542	A	19880222	199334	
KR 9210952	B1	19921224	KR 89777	A	19890125	199415	

Priority Applications (No Type Date): DE 3802025 A 19880125

Cited Patents: No-SR.Pub; 3.Jnl.Ref; EP 118828; EP 199946; JP 57044279; JP 58029187; US 4566063

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3802025	C		14		
EP 325677	A	G			
	Designated States (Regional): AT CH ES FR GB IT LI NL SE				
EP 325677	B1	G	26	G06F-009/38	
	Designated States (Regional): AT CH ES FR GB IT LI NL SE				

KR 9210952 B1 G06F-013/38

Abstract (Basic): DE 3802025 C

The buffer memory control allows command words from a main memory (MEM) to be loaded in the buffer memory (IBUF) in succession, with subsequent addressing of the stored commands via command addresses and transfer of the read commands to a command decoder (IDEC). An address **pipeline** (APL) controls the addressing of the buffer memory locations in response to the received loading addresses (FA), providing a delay which corresponds to the time required by a memory access control (MEMG) to access the memory in the given address sequence.

The distribution address is compared with the address locations of the commands already loaded in the buffer memory (IBUF) to allow decoding of each command.

ADVANTAGE - Allows use of large scale IC.

1/5

Title Terms: BUFFER; MEMORY; CONTROL; DATA; PROCESS; SYSTEM; ADDRESS; PIPE; CONTROL; ADDRESS; BUFFER; MEMORY; LOCATE; RESPOND; RECEIVE; LOAD; ADDRESS

Derwent Class: T01

International Patent Class (Main): **G06F-009/38 ; G06F-013/38**

International Patent Class (Additional): **G06F-012/08**

File Segment: EPI

12/5/23 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

003058646

WPI Acc No: 1981-F8682D/198126

Digital processor with pipeline **architecture - contains arithmetic unit of several independent circuits** performing **particular tasks independently**

Patent Assignee: AT & T TECHNOLOGIES INC (AMTT); WESTERN ELECTRIC CO INC (AMTT)

Inventor: BODDIE J R; THOMPSON J S

Number of Countries: 008 Number of Patents: 011

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
BE 887451	A	19810601				198126	B
GB 2069733	A	19810826	GB 814139	A	19810211	198135	
FR 2475763	A	19810814				198138	
NL 8100631	A	19810901				198139	
SE 8100735	A	19810914				198140	
DE 3104256	A	19820318				198212	
CA 1155231	A	19831011				198345	
GB 2069733	B	19840912				198437	
IT 1135394	B	19860820				198805	
SE 456051	B	19880829				198837	
DE 3104256	C	19910627				199126	

Priority Applications (No Type Date): US 80120059 A 19800211

Abstract (Basic): BE 887451 A

To improve the operating speed of a computer, the arithmetic unit comprises an assembly of circuits which **operate** independently, each **performing** a particular task. The tasks are **performed** during successive cycles with instructions flowing in **pipeline** fashion on a bus.

Instructions from a memory (100) are transferred to instruction registers (131-4) via a common control and data bus (101). A line memory (105) stores variable data words via a data register (106) and the data bus. Control circuits (131,211,212) decode the instruction words for processing sub units (112,115,116) during successive cycles of operation. This results in a data word which is transferred to an output **area** in the line memory. Auxiliary commands used on occasions ensure that the register contents are preserved during **execution** of a

program.
Title Terms: DIGITAL; PROCESSOR; PIPE; ARCHITECTURE; CONTAIN; ARITHMETIC; UNIT; INDEPENDENT; CIRCUIT; **PERFORMANCE** ; TASK; INDEPENDENT
Derwent Class: T01
International Patent Class (Additional): **G06F-003/00** ; **G06F-007/52** ; **G06F-009/38** ; **G06F-013/06** ; **G06F-015/20**
File Segment: EPI

```
Set     Items   Description
S1        738   LOOP? OR (ITERATIVE OR GROUP)()STATEMENT? OR PIPELIN? OR L-
            OOP()INVARIANT
S2       2246   RUNTIME OR RUN()TIME OR EXECUTION
S3      53799   PERFORM? OR WORK? OR FUNCTION? OR OPERATE?
S4      32683   CHECK? OR VERIFY? OR TEST? OR MEASURE? OR INSPECT? OR ANAL-
            YS? OR ANALYZ? OR EXAMIN? EVALUAT? OR INTERROGAT?
S5       8951   RANGE OR AREA OR REALM OR SCOPE OR SPHERE
S6         40   S1 AND S2
S7         19   S1 AND S3 AND S4 AND S5
S8          1   S6 AND S7
S9          1   S8 NOT PY>2001
File 256:SoftBase:Reviews,Companies&Prods. 82-2004/Apr
         (c)2004 Info.Sources Inc
```

9/5/1
DIALOG(R)File 256:SoftBase:Reviews,Companies&Prods.

01078131 DOCUMENT TYPE: Product

PRODUCT NAME: VIBE 1.0 (078131)

Institute for Computational Genomics Inc (716421)
263 McLaws Cir #200
Williamsburg, VA 23185 United States

RECORD TYPE: Directory

CONTACT: Sales Department

INCOGEN's Visual Integrated Bioinformatics Environment (VIBE) 1.0 is visualization and genomics discovery tool designed for the TimeLogic DeCypher platform. The client/server system, which **works** with TimeLogic's DeCypher accelerators, allows bioinformatics researchers to tap a broad **range** of data mining and discovery features. Using VIBE 1.0, researchers can tap drag-and-drop sequence **analysis** in **pipeline** construction. Users can also apply data filtering on simple or complex criteria. VIBE visualizes all DeCypher algorithms, streamlining processing. VIBE also offers research teams distributed, multi-user support options. The software's interface is navigated easily. Additionally, VIBE offers results from active and completed **pipelines** , and it provides with interactive or batch mode **pipeline execution** options. VIBE includes the Query, Search NT, Search AA, Target DB, Utility, Seals, and Visualization modules. The Search NT module contains similarity search algorithms using a nucleic acid (DNA) target database. Search AA uses an amino acid (protein) database. VIBE's Target DB module contains target database icons. The Utility module offers notification, multiple sequence alignment, and other features. VIBE's Seals is employed in standardizing sequence **analysis** protocols. VIBE allows researchers to **perform** their own sequence **analyses** , reducing data processing bottlenecks.

DESCRIPTORS: Bioinformatics; Data Mining; Genetics; Graphics for Science & Engineering; Laboratories; Research & Development; Science

HARDWARE: Hardware Independent
OPERATING SYSTEM: Open Systems
PROGRAM LANGUAGES: Perl; XML
TYPE OF PRODUCT: Mainframe; Mini; Micro; Workstation
POTENTIAL USERS: Bioinformatics, Biology Research
PRICE: Available upon request
REVISION DATE: 20020330

```
Set     Items   Description
S1     585430   LOOP? OR (ITERATIVE OR GROUP)()STATEMENT? OR PIPELIN? OR L-
            OOP()INVARIANT
S2     141836   RUNTIME OR RUN()TIME OR EXECUTION
S3    9466099   PERFORM? OR WORK? OR FUNCTION? OR OPERATE?
S4   12355827   CHECK? OR VERIFY? OR TEST? OR MEASURE? OR INSPECT? OR ANAL-
            YS? OR ANALYZ? OR EXAMIN? EVALUAT? OR INTERROGAT?
S5    3816246   RANGE OR AREA OR REALM OR SCOPE OR SPHERE
S6       9626   S1 AND S2
S7      22106   S1 AND S3 AND S4 AND S5
S8        586   S6 AND S7
S9      27969   S1 (3N) S3
S10    156805   S4 (3N) S5
S11         2   S6 AND S9 AND S10
S12   1771451   S4 AND S5
S13        51   S6 AND S9 AND S12
S14        51   S11 OR S13
S15        36   S14 NOT PY>2001
S16        34   S15 NOT PD>20010515
S17        32   RD (unique items)
File   8:Ei Compendex(R) 1970-2004/May W2
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/Apr
         (c) 2004 ProQuest Info&Learning
File 103:Energy SciTec 1974-2004/May B1
         (c) 2004 Contains copyrighted material
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/May W3
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/May W2
         (c) 2004 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/Apr W4
         (c)2004 Japan Science and Tech Corp(JST)
File   9:Business & Industry(R) Jul/1994-2004/May 14
         (c) 2004  The Gale Group
File  95:TEME-Technology & Management 1989-2004/May W1
         (c) 2004 FIZ TECHNIK
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
```

17/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04591188 E.I. No: EIP97013486448
Title: Adaptive loop scheduling algorithm on shared-memory systems
Author: Jin, Canming; Yan, Yong; Zhang, Xiaodong
Corporate Source: CSO Project (C/O), San Antonio, TX, USA
Conference Title: Proceedings of the 1996 8th IEEE Symposium on Parallel and Distributed Processing
Conference Location: New Orleans, LA, USA Conference Date: 19961023-19961026
Sponsor: IEEE
E.I. Conference No.: 45782
Source: IEEE Symposium on Parallel and Distributed Processing - Proceedings 1996. IEEE, Los Alamitos, CA, USA,96TB100088. p 250-257
Publication Year: 1996
CODEN: PSPDF8 ISSN: 1063-6374
Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review); T; (Theoretical)
Journal Announcement: 9702W4
Abstract: Using **runtime** information of load distributions and processor affinity, we propose an adaptive scheduling algorithm and its variations from different control mechanisms. The proposed algorithm applies different degrees of aggressiveness to adjust **loop** scheduling granularities, aiming at improving the **execution performance** of parallel **loops** by making scheduling decisions that match the real workload distributions at **runtime** . To **verify** the effectiveness of the algorithm and its variations, we implemented them on the KSR-1 and on the Convex Exemplar. We experimentally compared the performance of our algorithm and its variations with several existing scheduling algorithms on the two machines. The kernel application programs we used for performance evaluation were carefully selected for different classes of parallel **loops** . Our results show that using **runtime** information to adaptively adjust scheduling granularity is an effective way to handle **loops** with a wide **range** of load distributions when no prior knowledge of the **execution** can be used. The overhead caused by collecting **runtime** information is insignificant in comparison with the performance improvement. Our experiments show that the adaptive algorithm and its five variations outperformed the existing scheduling algorithms. (Author abstract) 7 Refs.
Descriptors: *Distributed computer systems; Storage allocation (computer); Adaptive algorithms; Decision theory; Computer simulation; Data communication systems; Synchronization
Identifiers: Shared memory system; Adaptive **loop** scheduling algorithm
Classification Codes:
722.4 (Digital Computers & Systems); 722.1 (Data Storage, Equipment & Techniques); 922.2 (Mathematical Statistics); 723.5 (Computer Applications)
722 (Computer Hardware); 723 (Computer Software); 921 (Applied Mathematics); 922 (Statistical Methods)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

17/5/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03106942 E.I. Monthly No: EIM9108-038972
Title: Design and performance of a small two-axis high-bandwidth steering mirror.
Author: Loney, Gregory C.
Corporate Source: Massachusetts Inst of Technology, Lexington, MA, USA
Conference Title: Beam Deflection and Scanning Technologies
Conference Location: San Jose, CA, USA Conference Date: 19910225
Sponsor: SPIE; Soc for Imaging Sciences & Technology
E.I. Conference No.: 14638

Source: Proceedings of SPIE - The International Society for Optical Engineering v 1454. Publ by Int Soc for Optical Engineering, Bellingham, WA, USA. p 198-206
Publication Year: 1991
CODEN: PSISDG ISSN: 0277-786X
Language: English
Document Type: PA; (Conference Paper) Treatment: A; (Applications); T; (Theoretical); X; (Experimental)
Journal Announcement: 9108
Abstract: A two-axis, high-bandwidth, small-aperture steering mirror called the High Bandwidth Steering Mirror (HBSM) has been designed, fabricated, and **tested** . The mirror/mechanism prototype **functions** within a servo **loop** either scanning a field of view or tracking a radiation source. The design focused on elements making up the beam-steering mechanism: mirror, restoring flexures, actuators, position sensors, and encompassing housing, and the part each component plays in making a mechanical system suitable for high-bandwidth operation. Inclusion of a novel flexural support allows one-degree peak-to-peak angular stroke (shaft space) at low frequencies and a small-signal closed- **loop** bandwidth of up to 10 kHz without the usual mechanical resonance-induced **loop** instabilities. This increased bandwidth allows substantial rejection of a disturbance spectrum in the 10-1000 Hz **range** and **execution** of fast, complex scan patterns. Pointing accuracies of 0.2 mu rad have been achieved in the laboratory. Details of the mechanical design and fabrication issues as well as the control- **loop** implementation are discussed. **Test** data are presented along with reports of the mirror's performance in use as an extended sensor. (Author abstract) 7 Refs.
Descriptors: *MIRRORS--*Design; SERVOMECHANISMS; OPTICAL SYSTEMS; SENSORS
Identifiers: STEERING MIRRORS
Classification Codes:
741 (Optics & Optical Devices); 732 (Control Devices)
74 (OPTICAL TECHNOLOGY); 73 (CONTROL ENGINEERING)

17/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03026243 E.I. Monthly No: EIM9102-008900
Title: An experimental performance **study of a** pipelined **recursive query processing strategy.**
Author: Shao, J.; Bell, D. A.; Hull, M. E. C.
Corporate Source: Dept of Comput Sci, Univ of Ulster at Jordanstown, UK
Conference Title: Proceedings of the Second International Symposium on Databases in Parallel and Distributed Systems
Conference Location: Dublin, Irel Conference Date: 19900702
Sponsor: IEEE Computer Soc; ACM SIGARCH; Office of Naval Research; British Computer Soc; Irish Computer Soc
E.I. Conference No.: 14052
Source: Proc Second Int Symp Databases Parallel and Distrib Syst. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2895-1). p 30-43
Publication Year: 1990
ISBN: 0-8186-2052-8
Language: English
Document Type: PA; (Conference Paper) Treatment: X; (Experimental)
Journal Announcement: 9102
Abstract: The **run - time** performance of a strategy (previously proposed by the authors) for processing recursive queries in deductive database systems is studied. The algorithm, introduced informally by examples, is coded in occam2, and runs on a network of transputers. A wide **range** of recursive queries and database structures are used as benchmarks. Both the speedup factors achieved and the elapsed time spent by the strategy in answering recursive queries are **analyzed** . Experimental results show that it is possible to achieve significant performance improvements when queries are evaluated in parallel. These results provide insights into the success of this strategy in meeting the primary objective of focusing on relevant

data. 23 Refs.
Descriptors: DATABASE SYSTEMS; COMPUTER SYSTEMS, DIGITAL-- **Pipeline** Processing; COMPUTER PROGRAMMING--Algorithms
Identifiers: DEDUCTIVE DATABASES; RECURSIVE QUERIES; QUERY PROCESSING; OCCAM2
Classification Codes:
723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

17/5/4 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01811587 ORDER NO: AADAA-I3001427
Research on networked control systems
Author: Ye, Hong
Degree: Ph.D.
Year: 2000
Corporate Source/Institution: University of Maryland College Park (0117)
Director: Gregory C. Walsh
Source: VOLUME 62/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 453. 133 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL ; ENGINEERING, INDUSTRIAL ; ENGINEERING, MECHANICAL
Descriptor Codes: 0544; 0546; 0548
ISBN: 0-493-10057-1

When a control **loop** is closed via a serial communication channel, it is labeled a Networked Control System (NCS). The primary objective of NCS design is to efficiently use the finite bus capacity while maintaining good closed- **loop** control system **performance** . In this dissertation, the focus is on the problems related to scheduling network traffic. The controller is assumed to be designed in advance without considering the effect of the network. Various scheduling schemes are then proposed, analytically verified and compared via simulations with fixed controller designs. Here, the primary interest lies in the dynamic scheduling of network traffic; that is, developing protocols that decide at **runtime** which channel to transmit and which to block.

For wireline NCS, a new protocol called Try-Once-Discard (TOD) is introduced. This new protocol dynamically allocates network resources to information sources based on need. An analytical stability condition for wireline NCS with both single-packet and multiple-packet transmission is derived. The condition is valid for both dynamic scheduling (e.g., TOD) and static scheduling algorithms (e.g., token passing). Simulation results **verify** the analytical prediction and demonstrate that dynamic scheduling outperforms static scheduling.

For real-time traffic scheduling of the wireless NCS, we propose a new protocol - Prioritized CSMA/CA is proposed; this is based on the definition of IEEE 802.11 and the requirements of real-time control and monitoring. For the first time, several algorithms for scheduling the traffic of wireless NCS have been proposed and validated; that is, constant penalty scheme, estimated error order scheme and lag first order scheme. All algorithms (include static scheduler) are compared with each other via simulation and the results show again that dynamic scheduling outperforms static scheduling (e.g., fixed order polling).

Several experiments were conducted to **verify** the former theoretical **analysis** and simulation results. In the network-only experiment, plant and controller dynamics are simulated via a digital computer; sensor nodes are realized by smart distributed I/O board with a controller **area** network (CAN) interface; and the communication channel is realized by CAN hardware. The result shows that dynamic scheduling (TOD) outperforms static scheduling in a real network environment allowing multiple packet transmission. The theoretical and numerical results of NCS with one packet transmission is further validated by the wireline SISO system experiment on the process trainer PT326. Experiments on the wireless MIMO system ensures good system performance even under worst case; that is, with a static

Author: Ofelt, David James
Degree: Ph.D.
Year: 1999
Corporate Source/Institution: Stanford University (0212)
Adviser: John L. Hennessy
Source: VOLUME 61/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 446. 92 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL ; COMPUTER SCIENCE
Descriptor Codes: 0544; 0984

Performance estimation of computer systems is an important topic to a large number of people in the computer industry. Computer architects need to be able to study future machines, compiler writers need to be able to evaluate the compiler output before a machine exists, and developers need insight into the machine's performance in order to tune their code. There are many performance estimation techniques that **range** from profile-based approaches to full machine simulation. Detailed simulation is one of the most common methods for estimating performance. It suffers, however, from potentially long run times when simulating large applications using detailed processor models.

This thesis discusses a profile-based performance estimation technique that uses a lightweight instrumentation phase that runs in order number of dynamic instructions, followed by an **analysis** phase that runs in order number of static instructions. This technique accurately predicts the **performance** of several **pipelines** including a detailed out-of-order issue processor model while scheduling far fewer instructions than does full simulation. The difference between the predicted **execution** time and the time obtained from full simulation is only a few percent. An extension to the basic technique accurately predicts branch prediction and instruction cache effects, but fails to handle data cache effects. Reasons for this failure are given. This thesis illustrates how this approach improves on earlier profile based **analysis** methods especially for the more advanced processor **pipelines** and illustrates how future processor trends will need new approaches.

17/5/7 (Item 4 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01664017 ORDER NO: AAD99-04444
OPTIMIZING PARALLEL INPUT/OUTPUT USING ADAPTIVE FILE SYSTEM POLICIES (PORTABLE PARALLEL FILE SYSTEM)
Author: ELFORD, CHRISTOPHER LLOYD
Degree: PH.D.
Year: 1998
Corporate Source/Institution: UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN (0090)
Adviser: DANIEL A. REED
Source: VOLUME 59/08-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 4240. 187 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

Recent research in techniques for optimizing parallel input/output has shown that matching available file system policies to application access patterns and resource requirements can produce substantial performance improvements. However, parallel file system policy availability varies significantly across computation platforms. Similarly, parallel scientific access patterns and resource requirements vary not only across applications but also among phases within an application. Unfortunately, the potential **range** of policies and access patterns make an exhaustive search of the policy space for optimal combinations prohibitively expensive.

We propose a two phase optimization strategy that first applies factor **analysis** to identify the most effective policy combinations on a given platform. Second, at **run time** , it **performs** closed **loop** control to refine policies. Rather than requiring potentially millions of experiments

to identify an effective 'optimal' policy combination, factor **analysis** uses a reasonable number of experiments to identify an effective, though not provably optimal, policy. Having identified effective policies on a given platform, we automatically monitor access patterns and system performance at application **run time** and refine file system policy parameters as bottlenecks become evident.

We have implemented this approach via several extensions to the Portable Parallel File System (PPFS) **testbed** . Sensor metrics that summarize dynamic access pattern information and file system performance effectively guide adaptive policy selection, affording significant performance improvements over less adaptive optimization strategies. Our results with both parallel access pattern benchmarks and parallel scientific applications demonstrate the efficacy of our approach.

17/5/8 **(Item 5 from file: 35)**

01593083 ORDER NO: AAD97-29722

BOUNDING WORST-CASE DATA CACHE PERFORMANCE

Author: WHITE, RANDALL T.
Degree: PH.D.
Year: 1997
Corporate Source/Institution: THE FLORIDA STATE UNIVERSITY (0071)
Major Professor: DAVID B. WHALLEY
Source: VOLUME 58/04-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 1984. 71 PAGES
Descriptors: COMPUTER SCIENCE ; ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0984; 0544

Tightly predicting worst-case **execution** times (WCETs) of programs on real-time systems with caches is difficult. Whether or not a particular reference is in cache depends on the program's previous dynamic behavior. While much progress has been accomplished recently on predicting instruction cache performance of programs, bounding worst-case data cache performance is significantly more challenging. Unlike instruction caching, many of the data addresses referenced by load and store instructions can change during the **execution** of a program. This dissertation describes an automatic tool-based approach for statically bounding the worst-case data cache performance of large code segments. It also presents the work done to **verify** the validity of the computed bounds. The given approach works on fully optimized code, performs the **analysis** over the entire control flow of a program, detects and exploits both spatial and temporal locality within data references, produces results typically within a few seconds, and produces, on average, 30% tighter WCET bounds than can be predicted without **analyzing** data cache behavior.

The given method of timing **analysis** involves several steps. First, data flow **analysis** within an optimizing compiler is used to determine the bounded **range** of addresses of each data reference relative to a global symbol or activation record. Second, virtual address ranges are calculated from the relative address ranges by examining the order of the assembly data declarations and the call graph of the entire program. Third, the control flow of the program is **analyzed** to statically categorize the caching behavior of each data reference. Fourth, these categorizations are used when calculating the **pipeline performance** of sequences of instructions representing paths within the program. Finally, the **pipeline** path **analysis** is used to estimate the worst-case **execution performance** of each **loop** and **function** in the program.

Overall, this dissertation presents a comprehensive report on methods and results of worst-case timing **analysis** of data cache behavior and shows that such an **analysis** can lead to a significantly tighter worst-case performance prediction. The given approach is unique and provides a considerable step towards realistic worst-case **execution** time prediction of contemporary architectures and its use in schedulability **analysis** for real-time systems.

17/5/9 (Item 6 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01572254 ORDER NO: AAD97-27596
OPTIMIZING FORTRAN90D/HPF FOR DISTRIBUTED-MEMORY COMPUTERS
Author: ROTH, GERALD H.
Degree: PH.D.
Year: 1997
Corporate Source/Institution: RICE UNIVERSITY (0187)
Professor: KEN KENNEDY; NOAH HARDING
Source: VOLUME 58/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 1375. 154 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

High performance Fortran (HPF), as well as its predecessor FortranD, has attracted considerable attention as a promising language for writing portable parallel programs for a wide variety of distributed-memory architectures. Programmers express data parallelism using Fortran90 array operations and use data layout directives to direct the partitioning of the data and computation among the processors of a parallel machine.

For HPF to gain acceptance as a vehicle for parallel scientific programming, it must achieve high performance on problems for which it is well suited. To achieve high performance with an HPF program on a distributed-memory parallel machine, an HPF compiler must do a superb job of translating Fortran90 data-parallel array constructs into an efficient sequence of operations that minimize the overhead associated with data movement and also maximize data locality.

This dissertation presents and **analyzes** a set of advanced optimizations designed to improve the **execution** performance of HPF programs on distributed-memory architectures. Presented is a methodology for performing deep **analysis** of Fortran90 programs, eliminating the reliance upon pattern matching to drive the optimizations as is done in many Fortran90 compilers. The optimizations address the overhead of data movement, both interprocessor and intraprocessor movement, that results from the translation of Fortran90 array constructs. Additional optimizations address the issues of scalarizing array assignment statements, **loop** fusion, and data locality. The combination of these optimizations results in a compiler that is capable of optimizing dense matrix stencil computations more completely than all previous efforts in this **area** . This work is distinguished by advanced compile-time **analysis** and optimizations performed at the whole-array level as opposed to **analysis** and optimization **performed** at the **loop** or array-element levels.

17/5/10 (Item 7 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01247904 ORDER NO: AADMM-65542
IMPROVING THE PERFORMANCE OF A DSP MICROPROCESSOR ARCHITECTURE
Author: TAKEFMAN, MICHAEL
Degree: M.A.SC.
Year: 1990
Corporate Source/Institution: UNIVERSITY OF TORONTO (CANADA) (0779)
Source: VOLUME 30/04 of MASTERS ABSTRACTS.
PAGE 1443. 152 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544
ISBN: 0-315-65542-9

An exploration of a microprocessor architecture for Digital Signal Processing is presented. The exploration methodology is similar to the **analyses** used in the design of Reduced Instruction Set Computers.

. The proposed architecture is compatible with the Motorola DSP56000 microprocessor at the assembly code level, but employs greater **pipelining** to improve **performance** . High-level simulation of the 56000 and the intermediate experimental architectures is used to characterize the **execution** of a suite of benchmark programs. The profiling data is used to reorganize the architecture to improve performance.

The proposed architecture is shown to improve the performance by a factor in the **range** of 1.25 to 2.11 across the benchmarks on a per clock basis.

An implementation proposal for the architecture is presented that enumerates the additional resources required by the proposed architecture and includes floorplans for a VLSI implementation.

17/5/11 (Item 8 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

874261 ORDER NO: AAD85-02922
A CLASS OF CELLULAR COMPUTER ARCHITECTURES TO SUPPORT PHYSICAL DESIGN AUTOMATION (VLSI LAYOUT, INTEGRATED CIRCUIT, ROUTING)
Author: RUTENBAR, ROBIN ARTHUR
Degree: PH.D.
Year: 1984
Corporate Source/Institution: THE UNIVERSITY OF MICHIGAN (0127)
Source: VOLUME 45/12-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 3870. 205 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

Special computer architectures for design automation (DA) problems are a practical solution to manage the increasing complexity of designing large integrated systems. A class of cellular architectures is studied which is applicable to physical DA problems that are cellular in nature: problems well-represented on a cellular grid with strongly local **functional** dependencies. The Raster **Pipeline** Subarray (RPS) class is a systolic organization, the central features of which evolved historically in classical picture-processing applications. RPS-structured DA engines have several attractive engineering properties: transparent expansion of processing capacity with a linear **pipeline** , direct accommodation of large grids with the raster data format, and application to differing tasks with programmable **pipeline** stages.

This thesis studies routing and integrated circuit design rule **checking** in an RPS environment. An experimental hardware/software RPS environment is constructed around existing RPS hardware; tools are developed to support the design and debugging of large-scale RPS-based DA systems. Maze-routing is the major application of interest; a mapping of maze-routing algorithms onto an RPS **pipeline** is developed and its complexity **analyzed** . A progression of increasingly complex, fully functional routers is implemented in the prototype RPS environment to **verify** feasibility. Large-scale benchmarks and comparisons with software routers show significant speedups. Design rule **checking** is considered from an algorithmic viewpoint: it is shown that a formalism derived from picture-processing tasks provides an elegant conceptual and notational tool for mapping rules **checking** onto an RPS **pipeline** . Hardware implementations of some specifications are **analyzed** . These studies prove that existing RPS engines can be improved incrementally and gracefully: additional **pipeline** stages improve **execution** times. Experiments over a **range** of **pipeline** lengths, and extrapolations based on experimental **measurements** support this claim. From these experiments, detailed performance models and cost/performance metrics are developed, treated analytically, and rigorously optimized. These results are employed to deduce the necessary functionality and tradeoffs to design optimal RPS-structured DA engines.

17/5/12 (Item 9 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

769451 ORDER NO: AAD82-02867
SPECIALIZED ASYNCHRONOUS DISTRIBUTED PIPELINES
Author: SAPHIER, STEWART HARVEY
Degree: PH.D.
Year: 1981
Corporate Source/Institution: UNIVERSITY OF MARYLAND (0117)
Source: VOLUME 42/08-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 3368. 193 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL; COMPUTER SCIENCE
Descriptor Codes: 0544; 0984

This dissertation presents a solution to the collision problem of dynamic **pipelines** . A dynamic **pipeline** can execute various algorithms each of which will be executing different functions as defined by the algorithm's flow graph and the data being input. Dynamic **pipelines** therefore have the problem of collisions between the algorithms as they each try to execute the various functions. This collision problem is currently circumvented by requiring that the **pipelines** be synchronous. All **functions** must execute in a fixed amount of time. This dissertation describes a technique for building asynchronous **pipelines** . These asynchronous **pipelines** are also distributed **pipelines** in that the **functions** to be executed are distributed over the processors within the **pipeline** . A **function** can be executed in more than one processor, but once a processor starts to execute the function, it will completely execute that function.

Since the processors (which are themselves **pipelined**) can not execute every function, they are individually built to execute only those functions assigned to them. The **pipeline** itself is restricted to a specific **area** of applications such as signals **analysis** .

The manner in which the functions are distributed to the processors within he **pipeline** is by first calculating a utility coefficient for each function. The utility coefficients are then used by a distributed algorithm to distribute the functions to the processors. Security processors may be added to the **pipeline** to both improve throughput and enhance flexibility of the **pipeline** . Security processors allow for the arrival of functions that have **execution** distributions that differ from what was previously specified. The utility coefficient can also be used to calculate the maximum arrival rate (of **functions**) that the **pipeline** can accept. Given the actual arrival rate, the utility coefficients can be used to calculate the average contents of the **pipeline** , and also the average contents of each processor within the **pipeline** . Since the utility coefficients are fairly easy to determine (and are the basic tool in designing the **pipeline**) the **pipeline** designer is able to both build and study (through simulated models by using a simulator given in this dissertation) various asynchronous distributed **pipelines** without difficulty.

17/5/13 (Item 10 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

769094 ORDER NO: AAD82-01985
ON THE DESIGN OF HIGH PERFORMANCE DIGITAL ARITHMETIC UNITS
Author: FARMWALD, PAUL MICHAEL
Degree: PH.D.
Year: 1981
Corporate Source/Institution: STANFORD UNIVERSITY (0212)
Source: VOLUME 42/08-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 3336. 101 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

Several new algorithms for use for enhancing the **performance** of **pipelined** digital computers have been developed and evaluated. The design of a particular such computer embodying most of these algorithms is discussed in detail--the S-1 Mark IIA. The relationship and importance of the new algorithms to the overall performance of such a machine is **analyzed** .

An algorithm for the very rapid **pipelined** computation of medium precision approximations (about 30 bits for the Mark IIA) to elementary functions is described. This method uses table lookup and two parallel multiplications to triple the precision available from direct table lookup. Current RAM technology permits the effective use of this algorithm for non-trivial word sizes. The method is applied to reciprocal, square-root, exponential, logarithm, arctangent, sine, cosine, and the error function.

A floating-point addition algorithm which has a much shorter latency than previous approaches is developed and **analyzed** . This algorithm lends itself to the efficient simultaneous calculation of floating-point sums and differences, which is of great value computing FFTs and to other related algorithms. The algorithm resolves floating-point addition into one of two independent cases, each of which can be implemented in fewer logic gate delays than previous algorithms.

Previous techniques of sorting on **pipelined** machines are **analyzed** and a new algorithm based on Quicksort is developed. This new algorithm is significantly faster and simpler than previous **pipelined** sorting techniques.

The use of skewed data representations to increase the performance of interleaved memories for many algorithms is well known. However a large price is paid in convenience by the use of such techniques. A new approach which allows the use of normal data representations but which has all of the performance advantages of the skewed representations is described. This technique is particularly valuable since the hardware used to implement it can also serve as a queue to minimize the effects of temporary stoppages in the instruction and operand fetching and arithmetic **execution** hardware.

Several other new techniques for performance enhancement are also described and **analyzed** , and fruitful directions for future work in this **area** are discussed.

17/5/14 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec

01466213 EDB-84-164019
Title: Transportation/Construction work above or near a pipeline
Author(s): Giraud Dagay, F.
Affiliation: Pipeline Serv.
Source: Pet. Tech. (France) v 262. Coden: PETED
Publication Date: May 1979
p 56-62
Document Type: Journal Article
Language: French
Journal Announcement: EDB8304
Country of Origin: France
Abstract: A discussion of the regulations and safety **measures** regarding construction or repair work on, or in the vicinity of, an operating oil **pipeline** , which could damage the **pipeline** covers administrative procedures that should precede the **execution** of the work; general rules for the construction of oil or gas **pipelines** , cables, tunnels and the like in parallel or crossing an existing **pipeline** or of railroads or highways above a **pipeline** ; and recommendations for the protection of the existing **pipelines** during the **work** , including methods for locating and uncovering buried **pipelines** and protecting the **work area** , the use of explosives, and examination of the **pipeline** and restoration of the **area** after the completion of the work.
Major Descriptors: CONSTRUCTION -- SAFETY STANDARDS; * **PIPELINES** --

. CONSTRUCTION
Descriptors: EXCAVATION; PETROLEUM; REGULATIONS
Broader Terms: ENERGY SOURCES; FOSSIL FUELS; FUELS; STANDARDS
Subject Categories: 022000* -- Petroleum -- Transport, Handling, & Storage

17/5/15 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7153602 INSPEC Abstract Number: B2002-02-8360-202, C2002-02-3340H-259
Title: A novel 1 MHz digital pulse width modulator chip
Author(s): Patella, B.; Prodic, A.; Maksimovic, D.
Author Affiliation: Dept. of Electr. & Comput. Eng., Colorado Univ., Boulder, CO, USA
Conference Title: PCIM 2001 Power Electronics Conference. Presented at Powersystems World 2001 Conference and Exhibition p.471-8
Publisher: Intertech Publishing, Stamford, CT, USA
Publication Date: 2001 Country of Publication: USA viii+553 pp.
ISBN: 0 87288 799 5 Material Identity Number: XX-2001-00324
Conference Title: Proceedings of PCIM/HFPC 2001. Part of Power Systems World 2001 Show
Conference Date: 11-13 Sept. 2001 Conference Location: Rosemont, IL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: New Developments (N); Practical (P); Experimental (X)
Abstract: In this paper, we describe a digital pulse-width modulator (DPWM) capable of 8-bit resolution at the switching frequency of 1 MHz. The DPWM chip, which has been designed and fabricated in a standard digital CMOS process, has novel architecture and takes relatively small silicon **area** . The power consumption is also relatively low. The potential for high performance and low cost digital realization opens the possibility of outperforming standard analog controllers, while adding an array of advantages of digital technology: higher production yield, design-time or **run - time** programmability, reduction or elimination of external tuning components, implementation of more sophisticated control algorithms, improved system integration and diagnostics, etc. The DPWM chip has been experimentally **tested** . A low-power 1 MHz synchronous buck converter is **operated** as a closed- **loop** voltage regulator with a controller that consists of the DPWM chip and an Analog Devices ADMC-401 DSP system. The architecture and operation of the DPWM chip are described. The complete closed- **loop** controller implementation and experimental results are presented. (5 Refs)
Subfile: B C
Descriptors: closed **loop** systems; DC-DC power convertors; digital control; digital signal processing chips; PWM power convertors; switching circuits
Identifiers: digital pulse-width modulator; 8-bit resolution; switching frequency; digital CMOS process; relatively small silicon **area** ; power consumption; high performance; low cost digital realization; digital technology; **run - time** programmability; control algorithms; synchronous buck converter; closed- **loop** voltage regulator; Analog Devices ADMC-401 DSP system; closed- **loop** controller; 1 MHz; 1.8 V; 5 V
Class Codes: B8360 (Power convertors and power supplies to apparatus); B1210 (Power electronics, supply and supervisory circuits); C3340H (Control of electric power systems); C7420 (Control engineering computing); C5135 (Digital signal processing chips)
Numerical Indexing: frequency 1.0E+06 Hz; voltage 1.8E+00 V; voltage 5.0E+00 V

17/5/16 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6034996 INSPEC Abstract Number: C9811-5220-010

Title: Reconfigurable processor architectures exploiting high bandwidth optical channels

Author(s): Sakr, M.F.; Levitan, S.P.; Giles, C.L.; Chiarulli, D.M.

Author Affiliation: Dept. of Electr. Eng., Pittsburgh Univ., PA, USA

Conference Title: Proceedings. IEEE Symposium on FPGAs for Custom Computing Machines (Cat. No.98TB100251) p.275-6

Editor(s): Pocek, K.L.; Arnold, J.M.

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA

Publication Date: 1998 Country of Publication: USA x+344 pp.

ISBN: 0 8186 8900 5 Material Identity Number: XX98-02491

U.S. Copyright Clearance Center Code: 0 8186 8900 5/98/$10.00

Conference Title: Proceedings IEEE Symposium on FPGAs for Custom Computing Machines

Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Comput. Architecture

Conference Date: 15-17 April 1998 Conference Location: Napa Valley, CA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P)

Abstract: There is growing interest in studying the possibility of reconfigurable architectures as replacements for general purpose computing for certain application domains. Reconfigurable systems can take advantage of deep computational **pipelines** , **perform** concurrent **execution** and are inherently data flow in nature. Furthermore, these systems have the capability of 'on the fly' reconfiguration of all or portions of the hardware to represent all the functionality required to complete the **execution** of an application. However, these architectures suffer from slow **run time** reconfiguration (RTR) due to the fact that the configuration memory resides off-chip and hence requires high access latency. This disadvantage limits the system performance and the application domain in which reconfigurable systems could prove effective. To overcome slow RTR, recent approaches include on-chip configuration memory to cache the next possible configurations. This approach trades off die **area** for fast RTR which diminishes the processing power of the reconfigurable processor. The high cost of adding configuration cache, up to 50% of the die **area** , would considerably increase the number of hardware reconfigurations required compared to architectures without on-chip cache. This paper presents an alternative reconfigurable architecture which overcomes these limitations by exploiting high bandwidth optical channels. We develop a performance model to **analyze** and compare the performance of cache based RTR architectures, optical based RTR architectures and hybrid optical-cache based RTR architectures. (4 Refs)

Subfile: C

Descriptors: optical information processing; performance evaluation; reconfigurable architectures

Identifiers: reconfigurable processor architectures; high bandwidth optical channels; general purpose computing; computational **pipelines** ; concurrent **execution** ; **run time** reconfiguration; application domain; on-chip configuration memory; die **area** ; performance model; cache based RTR architectures; optical based RTR architectures; hybrid optical-cache based RTR architectures

Class Codes: C5220 (Computer architecture); C5470 (Performance evaluation and testing); C5270 (Optical computing techniques)

17/5/17 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

5684273 INSPEC Abstract Number: B9710-1295-021, C9710-5190-018

Title: Synthesis and optimization of a bit-serial pipeline kernel processor

Author(s): Madrenas, J.; Ruiz, G.; Moreno, J.M.; Cabestany, J.

Author Affiliation: Univ. Politecnica de Catalunya, Barcelona, Spain

Conference Title: Biological and Artificial Computation: From Neuroscience to Technology. International Work-Conference on Artificial and

Natural Neural Networks, IWANN'97. Proceedings p.801-10
Editor(s): Mira, J.; Moreno-Diaz, R.; Cabestany, J.
Publisher: Springer-Verlag, Berlin, Germany
Publication Date: 1997 Country of Publication: Germany xxi+1401 pp.
ISBN: 3 540 63047 3 Material Identity Number: XX97-01355
Conference Title: Biological and Artificial Computation: From Neuroscience to Technology. International Work-Conference on Artificial and Natural Neural Networks, IWANN'97. Proceedings
Conference Date: 4-6 June 1997 Conference Location: Lanzarote, Spain
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The design process of an 8-bit 32-processing-units serial **pipeline** VLSI modular processor **performing** the parallel **execution** of a kernel classifier recall phase is described. Starting from VHDL high-level modelling, after **verifying** the correct circuit behaviour by means of digital simulation, the circuit has been synthesized and mapped on a 0.7 micron CMOS technology. Both **area** and delay optimized syntheses are performed for each processor cell, selecting in each case the best solution. Taking advantage of the constant data flow of the **pipeline** architecture, a dynamic realization of the memory elements using tri-state standard cells is proposed. This reduces both the circuit **area** and delays, without losing the convenience of an automatic standard cell placement and routing. From synthesis results, a working frequency of about 300 MHz is expected. A parallel-serial interface reduces external clock frequency requirements, and thus matching the external frequency limitations with fast on-chip processing. (11 Refs)
Subfile: B C
Descriptors: circuit optimisation; CMOS digital integrated circuits; hardware description languages; integrated circuit design; microprocessor chips; neural chips; **pipeline** processing; VLSI
Identifiers: bit-serial **pipeline** kernel processor; 8-bit 32-processing-units serial **pipeline** VLSI modular processor; parallel **execution** ; kernel classifier recall phase; VHDL high-level modelling; digital simulation; 0.7 micron CMOS technology; constant data flow; tri-state standard cells; standard cell placement; standard cell routing; parallel-serial interface; external frequency limitations; neural network; 8 bit; 0.7 micron; 300 MHz
Class Codes: B1295 (Neural nets (circuit implementations)); B2570D (CMOS integrated circuits); B1265F (Microprocessors and microcomputers); C5190 (Neural net devices); C5290 (Neural computing techniques); C5220P (Parallel architecture); C5440 (Multiprocessing systems); C5130 (Microprocessor chips)
Numerical Indexing: word length 8.0E+00 bit; size 7.0E-07 m; frequency 3.0E+08 Hz

17/5/18 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5465337 INSPEC Abstract Number: C9702-5470-019
Title: An adaptive loop **scheduling algorithm on shared-memory systems**
Author(s): Canming Jin; Yong Yan; Xiaodong Zhang
Author Affiliation: CSO Project, San Antonio, TX, USA
Conference Title: Proceedings. Eighth IEEE Symposium on Parallel and Distributed Processing (Cat. No.96TB100088) p.250-7
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1996 Country of Publication: USA xv+618 pp.
ISBN: 0 8186 7683 3 Material Identity Number: XX96-03013
U.S. Copyright Clearance Center Code: 0 8186 7683 3/96/$05.00
Conference Title: Proceedings of SPDP '96: 8th IEEE Symposium on Parallel and Distributed Processing
Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Comput. Architecture; IEEE Comput. Soc. Tech Committee on Distributed Process.; IEEE Comput. Soc. Dallas Chapter
Conference Date: 23-26 Oct. 1996 Conference Location: New Orleans, LA,

USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: Using **runtime** information of load distributions and processor affinity, we propose an adaptive scheduling algorithm and its variations from different control mechanisms. The proposed algorithm applies different degrees of aggressiveness to adjust **loop** scheduling granularities, aiming at improving the **execution** **performance** of parallel **loops** by making scheduling decisions that match the real workload distributions at **runtime** . To **verify** the effectiveness of the algorithm and its variations, we implemented them on the KSR-1 and on the Convex Exemplar. We experimentally compared the performance of our algorithm and its variations with several existing scheduling algorithms on the two machines. The kernel application programs we used for performance evaluation were carefully selected for different classes of parallel **loops** . Our results show that using **runtime** information to adaptively adjust scheduling granularity is an effective way to handle **loops** with a wide **range** of load distributions when no prior knowledge of the **execution** can be used. The overhead caused by collecting **runtime** information is insignificant in comparison with the performance improvement. Our experiments show that the adaptive algorithm and its five variations outperformed the existing scheduling algorithms. (7 Refs)
Subfile: C
Descriptors: parallel programming; performance evaluation; processor scheduling; shared memory systems; synchronisation
Identifiers: adaptive **loop** scheduling algorithm; shared-memory systems; **runtime** information; load distributions; processor affinity; **execution** performance; parallel **loops** ; KSR-1; Convex Exemplar; kernel application programs; scheduling granularity; adaptive algorithm
Class Codes: C5470 (Performance evaluation and testing); C5440 (Multiprocessing systems); C5220P (Parallel architecture); C6150N (Distributed systems software); C6110P (Parallel programming)

17/5/19 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5147539 INSPEC Abstract Number: B9602-6320-014
Title: Optoelectronic radar receiver for real-time radar imaging
Author(s): Wasilousky, P.A.; Pape, D.R.; Carter, J.A., III; Sunderlin, T.A.
Author Affiliation: Photonic Syst. Inc., Melbourne, FL, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2562 p.44-55
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1995 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1995)2562L.44:ORRR;1-E
Material Identity Number: C574-95212
U.S. Copyright Clearance Center Code: 0 8194 1921 4/95/$6.00
Conference Title: Radar/Ladar Processing and Applications
Conference Sponsor: SPIE
Conference Date: 13-14 July 1995 Conference Location: San Diego, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: We have previously presented the architecture and basic analytic results and for a **functional** 1-D **pipelined** hybrid optical/digital processing concept capable of generating a target **range** -Doppler profile in real time. Here we address the fundamental system processing algorithm and hardware development issues in some detail. The approach to performing real-time phase correction of the individual **range** profiles is outlined, along with the basic system operational **runtime**

algorithms and system processing **pipeline** . A description of the receiver hardware and its component functionality in terms of the presented operational theory is given as well. (3 Refs)
Subfile: B
Descriptors: distance **measurement** ; Doppler radar; optical correlation; optoelectronic devices; **pipeline** processing; radar imaging; radar receivers
Identifiers: optoelectronic radar receiver; real-time radar imaging; **functional** 1-D **pipelined** hybrid optical/digital processing; target **range** -Doppler profile; system processing algorithm; hardware development issues; real-time phase correction; operational **runtime** algorithms; receiver hardware; optical processing; **range** -Doppler image; optical correlator; hybrid signal processing
Class Codes: B6320 (Radar equipment, systems and applications); B6140C (Optical information, image and video signal processing); B4200 (Optoelectronic materials and devices)

17/5/20 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

4514611 INSPEC Abstract Number: C9312-5220P-028
Title: An area -constrained scheduling algorithm for the synthesis of pipelined systems
Author(s): Jae Hwan Park; Hong Shin Jun; Sun Young Hwang
Journal: Journal of the Korea Information Science Society vol.20, no.6 p.862-71
Publication Date: June 1993 Country of Publication: South Korea
CODEN: HJKHDC ISSN: 0258-9125
Language: Korean Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: For the design of **pipelined** systems satisfying given **area** or time constraints, high level synthesis techniques are employed to allow the users to explore design space. This paper proposes a heuristic algorithm that **performs pipeline** scheduling under **area** constraints. The proposed algorithm generates the design satisfying a given **area** constraint, while optimizing the overall **execution** time. The algorithm tries to distribute to each partition evenly by employing the list scheduling algorithm enhanced with delay insertion capability. It also supports chaining, multi-cycling, and mutual exclusion. Experimental results show that the proposed algorithm generates an optimal design for several benchmark programs. (12 Refs)
Subfile: C
Descriptors: circuit layout CAD; delays; heuristic programming; **pipeline** processing; program **testing** ; scheduling
Identifiers: **area** -constrained scheduling algorithm; synthesis of **pipelined** systems; time constraints; high level synthesis techniques; heuristic algorithm; **pipeline** scheduling; **area** constraints; list scheduling algorithm; delay insertion capability; chaining; multicycling; mutual exclusion; optimal design; benchmark programs; circuit layout CAD
Class Codes: C5220P (Parallel architecture); C7410D (Electronic engineering); C5440 (Multiprocessor systems and techniques); C6150G (Diagnostic, testing, debugging and evaluating systems)

17/5/21 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

4506070 INSPEC Abstract Number: C9312-6130B-005
Title: Interactive volume rendering of large fields
Author(s): Sakas, G.
Author Affiliation: Fraunhofer-Inst. for Comput. Graphics, Darmstadt, Germany
Journal: Visual Computer vol.9, no.8 p.425-38

Publication Date: Aug. 1993 Country of Publication: West Germany
CODEN: VICOE5 ISSN: 0178-2789
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Presents the volume-rendering **pipeline** and the most typical of the existing methods for each **pipeline** stage. The complexity of each stage in terms of computing time is **analyzed** for each method. Then the demands and the **scope** of interactive volume rendering are briefly summarized. Based on this **analysis** , the author examines alternate solutions to optimize each **pipeline** stage in order to allow interactive visualization while maintaining the image quality. The proposed method maximizes interactive manipulation possibilities and minimizes runtimes by sampling at the Nyquist rate and by flexibly trading off quality for **performance** at any **pipeline** level. This approach is suitable for rendering large, scalar, discrete volume fields such as semi-transparent clouds (or X-rays) on the fly. (39 Refs)
Subfile: C
Descriptors: clouds; data visualisation; interactive systems; natural sciences computing; Nyquist criterion; optimisation; **pipeline** processing; rendering (computer graphics); X-rays
Identifiers: interactive volume rendering; discrete scalar volume fields; **pipeline** ; computing time; image quality; interactive manipulation; **runtime** minimization; Nyquist sampling; performance; semitransparent clouds; X-rays; large fields; scientific visualization
Class Codes: C6130B (Graphics techniques); C7300 (Natural sciences)

17/5/22 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00409497 JICST ACCESSION NUMBER: 87A0229207 FILE SEGMENT: JICST-E
Seismic reliability of buried pipeline **networks. No. 3.**
HAGIO AKIRA (1); SUZUKI NOBUHISA (1); OOBA SYUUKOU (1); KAMEMURA TOSHIHIKO (2); SUZUKI ISAMU (2)
(1) Nihonkokan Jukoken; (2) Nippon Kokan K.K.
Nippon Kokan Giho(Nippon Kokan Technical Report), 1987, NO.116, PAGE.53-60 , FIG.14, TBL.7, REF.11
JOURNAL NUMBER: F0229AAG ISSN NO: 0468-2815 CODEN: NPKGA
UNIVERSAL DECIMAL CLASSIFICATION: 628.14/.15+628.2 624.131.53/.55
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Probabilistic approach has been made for simulations of restoration **works** of a damaged **pipeline** network for gas distribution service by introducing the Markov process. A new approximate solution technique, Subnetwork Method, is proposed in order to evaluate connectivity between a supply node and a demand node, and quite effective for reduction of the computer **run time** . The damages **analyzed** are those of Sendai City caused by the Miyagiken-oki earthquake in 1978. The simulations conducted in this paper deal with the process of recovery of the network system from different aspects. They are evaluation of recovery rate of some subdivided areas and connectivity between the designated nodes during the restoration works. In consequence of the results of the simulations, it can be recommended that the restoration works should be started from the subdivided **area** in which the least amount of damages are observed.(author abst.)
DESCRIPTORS: **pipeline** (system); lifeline; seismic **analysis** ; mathematical model; gas service industry; seismic damage; disaster recovery; block(object); gas supply system; Markov process; CPM; network; Miyagi; buried pipe; town gas; reliability(property); evaluation; earthquake
BROADER DESCRIPTORS: pipe line; facility and building; structure **analysis** ; **analysis** ; model; industry; natural disaster; disaster; disaster countermeasure; countermeasure; recovery and reclamation; system; stochastic process; process; network programming; operations research; Tohoku District; Japan; East Asia; Asia; pipe classified by application

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Set     Items   Description
S1     797048   LOOP? OR (ITERATIVE OR GROUP)()STATEMENT? OR PIPELIN? OR L-
            OOP()INVARIANT
S2     357968   RUNTIME OR RUN()TIME OR EXECUTION
S3   13556462   PERFORM? OR WORK? OR FUNCTION? OR OPERATE?
S4    8548198   CHECK? OR VERIFY? OR TEST? OR MEASURE? OR INSPECT? OR ANAL-
            YS? OR ANALYZ? OR EXAMIN? EVALUAT? OR INTERROGAT?
S5    6009656   RANGE OR AREA OR REALM OR SCOPE OR SPHERE
S6       6335   S1 (S) S2
S7       4165   S1 (S) S3 (S) S4 (S) S5
S8         91   S6 (S) S7
S9         69   S8 NOT PY>2001
S10        61   S9 NOT PD>20010515
S11        40   RD (unique items)
File  15:ABI/Inform(R) 1971-2004/May 17
         (c) 2004 ProQuest Info&Learning
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         (c) 1999 Business Wire
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         (c) 1999 The Gale Group
File 553:Wilson Bus. Abs. FullText 1982-2004/May
         (c) 2004 The HW Wilson Co
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and service excellence, is a leading supplier of high- **performance** , Web-based computing solutions which help enterprises compete in the global marketplace. Digital gives its customers a...

11/3,K/38 (Item 1 from file: 813)
DIALOG(R)File 813:PR Newswire

0865430 SJ007
SYMANTEC DELIVERS IMPROVED SPEED PERFORMANCE IN ENTERPRISE DEVELOPER 2.5

DATE: October 2, 1995 07:57 EDT WORD COUNT: 527

...database engines; a new report generator, Crystal Reports; Informix Data Link; and a message customizer.

In benchmark **testing** , Coordinated Digital Systems, a Charlotte-based consulting group, found Enterprise Developer to be substantially faster than Version 2.0 in the main **tested** categories. "The browse **performance** was particularly impressive," said Pete Griffiths, president of CDS. "This is the **area** that is critical to our application development and Enterprise Developer **performed** better than any other product we evaluated." The results of these **tests** indicated that the query speed retrieval rates increased 500%, from 2,860 to 15,400 records in 60 seconds and SCALEScript **execution** speed doubled, resulting in a 50% speed reduction time for **loop testing** .

"We are very pleased with this new version of Enterprise Developer," said Ted Schlein, vice president of...

11/3,K/39 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04532168 Supplier Number: 46659432 (USE FORMAT 7 FOR FULLTEXT)
Single-board Machine Vision for OEMs
News Release, pN/A
August 28, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 542

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...is capable of issuing and retiring as many as three instructions per clock cycle, using five independent **execution** units. The 603e can execute a single precision floating-point multiply and add operation in every clock ...

...operating system that supports multi-tasking and yields fast context switching tunes. mvPower includes Datacube's powerful **pipeline** processing architecture, which pipes video data through a configurable series of sequentially connected computational elements. Each of these elements optimizes the **performance** of a specific image processing task. Multiple parallel **pipelines work** synchronously to further enhance data throughput. mvPower's AU element -- a built-in arithmetic processor and crosspoint...

...three VSIM memories which, in addition to storing images in memory, are capable of certain image processing **functions** . Each of Datacube's VSIM modules has a crosspoint switch, statistical processor, LUT, ALU, and feature extractor...

...MaxACQ modules provide high throughput and simplify integration for a variety of analog and digital sensors including **area** , line-scan, and TDI

types in a **range** of resolutions. The basic MaxACQ module on mvPower has two 4: I camera multiplexers and supports simultaneous...

...easy-to-use, the tools support image acquisition, preprocessing, object finding (normalized gray-scale correlation or blob **analysis**), metrology, and camera calibration. The stand-alone mvPower image processing engine simplifies integration and improves **performance** in a wide variety of applications including SMD placement, wire bonding, die bonding, robot guidance, label **inspection** , and more. Dr. Scott Roth, Vice President, Datacube's Machine Vision Group, explains "our target market for mvPower is OEMs who need motion guidance, accurate **measurement** , and fast **inspection** in their machines, and our volume pricing has been set to attract them." Founded in 1979, Datacube...

...of image processing hardware, software, and systems designed to meet technology and business requirements of a wide **range** of scientific and commercial users. Datacube is a primary supplier to Fortune 100 firms and major research...

11/3,K/40 (Item 1 from file: 160)
DIALOG(R)File 160:Gale Group PROMT(R)

02246882
Computer Products Introduces LAN Compatible RTP
News Release March 2, 1989 p. 1

Computer Products, Inc. **Measurement** & Control Division has introduced an intelligent network product which interfaces their analog and digital I/O product family, RTP, with Local **Area** Network environments. Named G-2 LAN Compatible RTP, it will offload a host computer by providing full preprocessing capability, including such features as scanning, engineering units conversion, calculations, sequence of events, and closed **loop** control. G-2 will initially **operate** in a DECnet/Ethernet environment. Based on Motorola 68020/68881 technology, G-2 is a 19-inch...

... aocommodation for up to three Input/Output Bus Converters. The G-2 processor card combines a high **performance** 68020 CPU with a 68881 Floating Point Coprocessor, each running at 16 MHz, for extremely fast instruction **execution** . The 256 Kbyte ROM contains the Executive and Database Compiler while the **Run Time** code and Sequence of Events data are stored in 1 Mbyte of onboard dynamic RAM.
...